

SILICON-BASED MILLIMETER-WAVE FRONT-END DEVELOPMENT FOR MULTI-GIGABIT WIRELESS APPLICATIONS

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SILICON-BASED MILLIMETER-WAVE FRONT-END DEVELOPMENT FOR MULTI-GIGABIT WIRELESS APPLICATIONS

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My Late Mother:

For her blessings and teachings.

My Father:

For his teachings, support, and sacrifices.

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Summary

With rapid advances in semiconductor technologies and packaging schemes, wireless products have become more versatile, portable, inexpensive, and user friendly over last few decades. However, the ever-growing demand of consumers to share information efficiently at higher speeds requires higher data rates, increased functionality, lower cost, and more reliability. The 60-GHz-frequency band, with 7 GHz license-free bandwidth addresses, such demands, and promises a low-cost multi-Gbps wireless transmission with a power budget in the order of 100 mW.

This dissertation presents the systematic development of key building blocks and integrated 60-GHz-receiver solutions. Two different approaches are investigated and implemented in this dissertation: (1) low-cost SiGe-based direct-conversion low-power receiver front-end utilizing gain-boosting techniques in the front-end low-noise amplifier, and (2) CMOS-based heterodyne receiver front-end suitable for high-performance single-chip 60 GHz transceiver solution. The ASK receiver chip, implemented using 0.18 μm SiGe, presents a complete antenna-to-baseband multi-gigabit 60 GHz solution with the lowest reported power budget (25 pJ/bit) to date. The subharmonic direct conversion front-end, implemented using 0.18 μm SiGe, presents excellent conversion properties with a 4 GHz DSB RF bandwidth. On the other hand, the CMOS heterodyne implementation of the 60 GHz front-end receiver, targeted towards a robust, single-chip, high-performance, low-power, and integrated 60 GHz transceiver solution, presents the most wideband receiver front-end reported to date. Finally, different multi-band and tunable millimeter-wave circuits are presented towards the future implementation of cognitive and multi-band millimeter-wave radio.

Chapter 1

Introduction

1.1 Motivation

There has been tremendous growth in wireless technologies over the last few decades. One significant aspect of this growth is the evolution of personal-communication devices, such as cell phones, music players, personal digital assistants (PDAs), laptops with communication capabilities, wireless security systems, wireless storage systems, and global positioning systems (GPS). With rapid advances in semiconductor technologies and packaging schemes, products have become more versatile, portable, inexpensive, and user friendly. However, the ever growing demand of consumers to share information efficiently at higher speeds than what is possible using current technologies, requires higher data rates, increased functionality, lower cost, and more reliability. This increasing challenge for a superior performance at a lower cost is driving the need for new communication standards and efficient communication schemes.

1.1.1 Different wireless communications schemes

The term wireless normally refers to any type of electrical or electronic operation accomplished without the use of a *hard-wired* connection. If desired, these may be accomplished with the use of wires [1]. Personal-communication devices mostly use the

air as the communication medium. However, the omni-directional nature of the medium requires that certain rules or standards be followed to reduce conflicts between different communication devices. The Federal Communications Commission (FCC) regulates wireless communications in the United States by allocating frequencies and setting regulations to be followed for different wireless communication schemes. A limited selection of such standards is summarized in Table 1.1.

Table 1.1. Comparison of different wireless communication standards.			
Standard	Frequency	Data rate	Distance
CDMA	824-849 MHz 869-894 MHz	Less than 1 Mbps	Greater than 1mile
GSM	880-915 MHz 925-960 MHz	Less than 1 Mbps	Greater than 1mile
GPS	1.575 GHz	Very slow	Greater than 1mile
WCDMA	Around 2 GHz	2 Mbps	Greater than 1mile
Bluetooth	2.402-2.408 GHz	3 Mbps	10 meters
802.11b/g	2.4-2.483 GHz	11 Mbps @802.11b 54 Mbps@ 802.11g	35 meters (indoor)
802.11a	5.15-5.35 GHz 5.47-5.725 GHz 5.725-5.875 GHz	54 Mbps	30 meters (indoor)
UWB	3-10 GHz	Up to 1 Gbps	3-10 meters depending on the transmission speed

The critical aspects of a wireless standard are the span of the wireless channel and the data throughput. These aspects are typically determined by the requirements of a particular application. The traditional cellular standards, e.g., a global system for mobile communication (GSM), code division multiple access (CDMA), and wideband code division multiple access (WCDMA), have throughputs from tens of kbps to approximately 1-2 Mbps. This throughput is sufficient for communication in terms of the voice, limited data-transfer, and limited image-transfer applications over a few miles

(base station to user). The personal-area-networking standards, e.g., Bluetooth and HomeRF, are typically used to support cellular devices or other applications that require a less than 1-3 Mbps data rate in an indoor environment; i.e., a transmission range of less than 10 m. These standards have demands similar to the cellular market in terms of cost, size, and portability. On the other hand, IEEE802.11a/b/g standards typically support data transfer in an indoor environment; e.g., wireless Internet and wireless networking of a set of computers. When compared to Bluetooth and HomeRF, IEEE802.11a/b/g standards provide a much higher throughput (11 Mbps for 802.11b, 54 Mbps for 802.11a/g, and 250 Mbps for 802.11n) to support the data-transfer requirements. Ultra-wide-band (UWB) communications have increased the data rate up to hundreds of Mbps over a distance up to 10 m [2]. Applications of such a UWB scheme are high-speed personal area networking (PAN), short-range imaging, short-range and high-speed radios, radar, and military communications. However, the capacity of hard drives (up to terabytes), memory, and other storage devices is increasing exponentially as depicted in Figure 1.1.

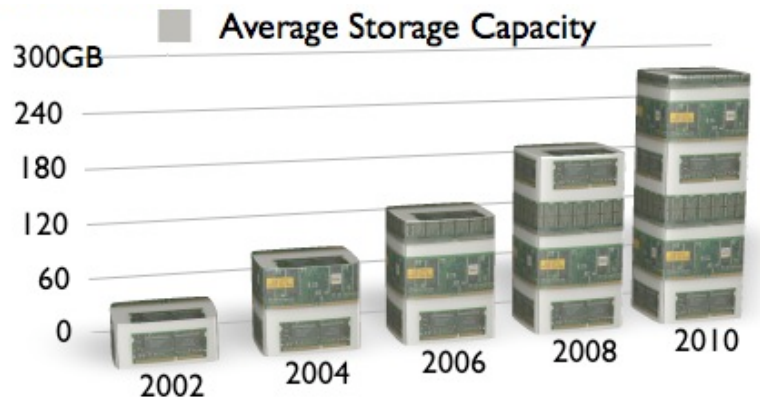


Figure 1.1. The predicted average storage capacity of hard drives.

In addition, the wired-multimedia standards, e.g., the peripheral component interconnect (PCI), unified display interface (UDI), and high-definition multimedia interface (HDMI), have throughput specifications of more than 1-10 Gbps. Hence, UWB cannot satisfy either the multimedia applications, or the multi-gigabit-data-transfer requirements.

1.1.2 Multi-gigabit radio

There are two alternatives to enhance the data rate of a wireless communication scheme. The first alternative requires a bandwidth-efficient modulation scheme. The second alternative requires a large bandwidth to support a large throughput using simple modulation schemes. The spectral efficiency, i.e., the data rate per bandwidth, of different modulation schemes in bps/Hz is shown in Figure 1.2.

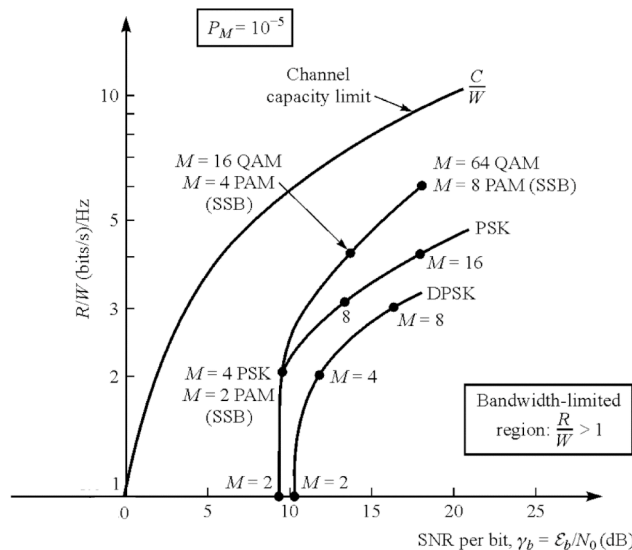


Figure 1.2. Spectral efficiency of different modulation schemes for a bit-error rate of 10^{-5} .

As shown in Figure 1.2, the signal-to-noise ratio (SNR) requirement of a modulation scheme for a particular bit-error rate (BER) increases with the increased spectral efficiency. Currently, many research efforts at RF frequencies (mostly 2.4 GHz and 5.8

GHz) focus on improving the spectral efficiency of the communication schemes by increasing the complexity of the baseband processors. Advances in semiconductor IC processes facilitate such efforts to improve the performance of the transceiver. Multiple-input-multiple-output (MIMO) systems are shown to improve the capacity of 802.11n schemes as shown in Figure 1.3. However, the wireless bandwidths at those frequency bands, on the order of 100 MHz, limit the data rate of such schemes. Among the communication schemes shown in Table 1.1, UWB has the advantage of a large bandwidth (7 GHz) to support a greater than 1 Gbps data rate. However, the *ultra-wide-band* nature of the fractional bandwidth (bandwidth/center frequency) of this frequency band complicates the system development. In addition, the FCC strictly regulates the transmitter power (at -41.3 dBm/MHz) at UWB frequencies to minimize the interference with the existing 802.11a standard. Figure 1.3 summarizes the trend of different wireless communication schemes and the multimedia trend.

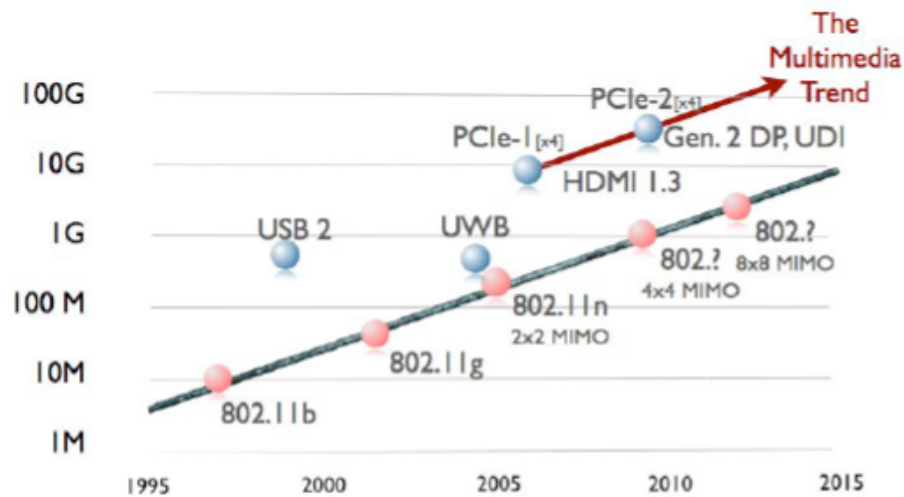


Figure 1.3. Trend of multimedia standards and wireless communication standards.

From the trend, it is obvious that the conventional wireless communication standards (IEEE802.11n and UWB) are one generation behind the corresponding *wired*-multimedia standards; i.e., the data rate of the future IEEE802.11n/UWB schemes are one order of magnitude lower than that of the wired-multimedia schemes.

On the other hand, the worldwide-license-free 59-64 GHz band (59-66 GHz band in Japan and Europe, 57-64 GHz band in USA) [3] has a sufficiently large bandwidth to reach a multi-gigabit throughput using simple modulation schemes; e.g., amplitude-shift keying (ASK) and binary phase-shift keying (BPSK). The advanced modulation schemes, e.g., quadrature phase-shift keying (QPSK) and quadrature amplitude modulation (QAM), can enable data rates higher than 10 Gbps. Hence, the potential data rate of the 60 GHz schemes are similar to the multimedia standards, and thus, a seamless communication scheme can be achieved. The 60 GHz frequency band (a synonym for the 59-64-GHz-frequency band) is still narrowband (the fractional bandwidth being less than 10%), and the standard direct-conversion or super-heterodyne system architectures can be utilized.

1.1.3 60 GHz communications system

There are several chip-level, package-level, and system-level design challenges for the implementation of 60 GHz communication systems. The significant attenuation in the wireless channel at 60 GHz [4] is one of the most critical challenges of 60 GHz radios. The direct-path loss is measured to be approximately 68 dB at 1 m distance, and this loss increases by 6 dB when doubling the distance. In addition, any object between the transmitter and the receiver would also increase the loss of the channel significantly.

Other important aspects of 60-GHz-radio design are the integration of the IC

process and the packaging platform. Silicon-based technologies have inherent advantages over commercial III-V compound-semiconductor technologies. Lower processing costs, higher yields, and larger infrastructural investments are collectively responsible for the lower-cost-per-die-area on silicon substrates. The system-on-chip (SoC) integration is the ultimate solution for communications systems. This approach significantly reduces the number of external components and the cost and size of the radio. Silicon-germanium BiCMOS and CMOS are the only feasible technologies to realize SoC solutions for 60 GHz radios. Complete monolithic SoC integration requires the implementation of low-power design techniques to minimize the power consumption of 60 GHz chips.

Another important aspect of system integration is the module integration and packaging. A compact module is required to integrate new 60 GHz systems to existing multimedia products. A low-cost realization of a high-gain, compact printed antenna is required. In addition, the interconnection between the chip and the package is critical in terms of loss, reliability, and matching. Given these challenges, a convergent system approach, as discussed later in this thesis, is necessary for the multi-gigabit system implementation using the 60 GHz frequency band.

1.2 **Organization of the thesis**

This dissertation is organized as follows. The second chapter summarizes the approach for the realization of the 60 GHz wireless systems, in terms of the circuits, building blocks, and integration. The traditional millimeter-wave system approach is revisited to distinguish it from the approach presented here. The reported system approach marks a true convergence of low-cost integrated IC development, low-cost packaging, and low-power signal processing requirements. The link budget and the system architectures of a portable 60 GHz wireless system are analyzed in the second chapter. Finally, a hybrid-integration concept is demonstrated through the development of a 4X sub-harmonic mixer using a low-cost organic platform. The hybrid approach acts as the link between the traditional approach and the integrated low-cost approach.

The third chapter presents the development of direct-conversion 60 GHz receiver front-ends using the 0.18 μm and 0.12 μm silicon-germanium (SiGe) hetero-junction bipolar transistor (HBT) IC processes. The implementation of a high-gain front-end amplifier is essential for a direct-conversion front-end. However, to realize the gain specifications using the low-cost 0.18 μm SiGe HBT process, a novel gain-boosting technique for millimeter-wave cascode amplifiers is proposed and analyzed. A sub-harmonic-mixing scheme and a diode-based non-coherent amplitude-detection scheme are presented. Finally, the integrated 60 GHz multi-gigabit receivers in 0.18 μm SiGe are demonstrated using amplitude-detection and subharmonic schemes. The non-coherent ASK receiver shows the lowest reported power budget (25 pJ/bit) from the antenna to the demodulated baseband. The subharmonic front-end demonstrates a conversion gain of 16 dB with 4 GHz RF bandwidth for only 27 mW DC power consumption.

The fourth chapter introduces the CMOS technology as a solution for 60 GHz communications systems in terms of a lower cost and a higher integration perspective. Characteristics of the CMOS transistors and the passive devices, e.g., transmission lines and capacitors, are investigated to determine the suitable architecture for the receiver front-end. A robust super-heterodyne scheme is proposed to maximize the speed, performance, and reliability of the receiver front-end. A systematic development of the front-end amplifier is presented in this chapter. In addition, the single-ended and differential front-end mixing schemes are implemented and compared. Finally, an integrated front-end receiver is presented using a 90 nm CMOS process.

The fifth chapter discusses stand-alone millimeter-wave tunable circuits that can be useful for multiband applications. A multilayer, compact directional filter structure is proposed towards a multiband filtering solution. The design strategy of a frequency-tunable low-noise amplifier is demonstrated to realize a millimeter-wave multiband or cognitive system.

The unique contributions of this research are summarized in the sixth chapter. At the end, the future research directions are presented.

Chapter 2

Overview of 60 GHz System

2.1 Introduction

This chapter revisits the traditional approach for the 60 GHz system development. Three major aspects of the system realization are circuits, module, and integration. A convergent approach is presented towards a low-cost, low-power system development in terms of front-end ICs, module, and signal-processing requirements. Different system architectures are described to determine the suitable one for 60 GHz systems. In addition, the link budget and the frequency planning are also analyzed. Finally, a hybrid integration concept is demonstrated using a low-cost organic platform. The hybrid approach acts as the link between the traditional approach and the integrated low-cost approach suitable for a portable 60 GHz system.

2.2 Background

The history of the 60 GHz systems can be traced back to early demonstrations by Sir J. C. Bose in 1895 using semi-conducting crystals [5]. In 1950s, long-haul communications using buried circular waveguides are developed by Bell Labs. In the later part of the twentieth century, 60 GHz frequency band is utilized in only military communications. Point-to-point wireless systems operating at 60 GHz have been used for many years by the intelligence community for high security communications and by the military for satellite-to-satellite communications. Their interest in this frequency band stems from the oxygen absorption of the electromagnetic energy at 60 GHz. This absorption occurs to a much higher degree at 60 GHz than at lower frequencies typically used for wireless communications. This absorption weakens (attenuates) 60 GHz signals over distance, so that signals cannot travel far beyond their intended recipient. For this reason, 60 GHz is an excellent choice for covert satellite-to-satellite communications because the earth's atmosphere acts like a shield preventing earth-based eavesdropping. Another consequence of O₂ absorption is that radiation from one particular 60 GHz radio link is quickly reduced to a level that will not interfere with other 60 GHz links operating in the same geographic vicinity. This reduction enables higher *frequency reuse*, i.e., the ability for more 60 GHz links to operate in the same geographic area than links with longer ranges. Also, the 60 GHz links are far more secure given their limited range. However, with the increasing potential of low-cost, portable 60 GHz applications, there is an evolution and convergence in terms of IC process and module integration.

2.2.1 Evolution of IC process

Historically, gallium-arsenide (GaAs) pseudomorphic-high-electron-mobility transistor (pHEMT), GaAs metamorphic-high-electron-mobility-transistor (MHEMT), GaAs HBT, indium-phosphide (InP) HBT, InP pHEMT, and indium-gallium-arsenide (InGaAs) pHEMT are used as the IC processes for millimeter-wave integrated circuits [6]-[8]. However, silicon-based technologies have inherent advantages over the commercial III-V compound semiconductor technologies in terms of processing cost and integration of the RF front-end with the baseband circuitry. Silicon's real strength lies in its system-on-chip (SoC) integration capability. GaAs and InP technologies lag far behind silicon-based technologies in terms of device density, integration, and yield [9].

The primary performance parameters of an IC process are denoted by f_T (unity current-gain cutoff frequency) and f_{\max} (maximum frequency of oscillation). f_T is mostly independent of device parasitics, and do not consider matching conditions. However, f_{\max} considers device-layout parasitics, and determines the absolute maximum frequency of operation of a device [10]. In a CMOS process, the high sheet resistance of the polysilicon gates increases resistive losses, and the lossy substrate increases substrate-coupling losses. Furthermore, the large gate-to-source capacitance limits the high-frequency performance of CMOS devices. However, the high-frequency performance of CMOS devices is enhanced with the reduction in the channel length of transistors (130 nm, 90 nm, 65 nm, 45 nm, and so on) [10].

The introduction of silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) further enhanced the potential of silicon-based processes [11]. SiGe HBTs have a much higher mobility, and hence, transit times are reduced, resulting in higher f_T and f_{\max} .

Figure 2.1 shows the typical f_T of CMOS and SiGe HBT transistors at different technology nodes.

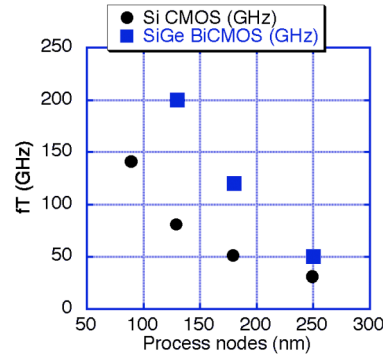


Figure 2.1. Typical f_T of CMOS and SiGe HBT devices at different technology nodes.

The lossy silicon substrate, present in both of these technologies, requires proper shielding of interconnects. In addition, thick metal layers are incorporated in these IC processes to reduce the resistive loss of interconnects and matching networks. Lumped inductive components cannot be used at millimeter-wave frequencies. Hence, shielded transmission lines (microstrip, coplanar waveguide (CPW), or conductor-backed coplanar waveguide (CB-CPW)) are implemented. However, a low power, low noise, and wideband implementation of the 60 GHz front-end (LNA, mixer, oscillator etc.) remains a challenge to designers. It might require different circuit techniques for different building blocks (e.g., gain-boosting in amplifiers, resonance/tuning in amplifiers and mixers etc.), especially when using the lower-end HBT or CMOS processes (much cheaper when compared to the state-of-the-art HBT of CMOS processes); e.g., 0.18 μm SiGe HBT and 0.13 μm CMOS processes.

2.2.2 Evolution of module integration

Historically, the 60 GHz modules are bulky, expensive, and used for military applications. Figure 2.2 shows the photograph of a traditional 60 GHz module for point-to-point data transfer.



Figure 2.2. Photograph of the traditional 60 GHz point-to-point communication system.

Traditionally, stand-alone millimeter-wave components, e.g., waveguide, horn antenna, and traveling-wave amplifiers are utilized in a 60 GHz system. Hence, the system is not portable as shown in Figure 2.2. For commercial applications, the trend has been to realize printed antenna and planar transmission lines (microstrip or CPW) to reduce the size and cost and to increase portability. The number of external components has been reduced with the help of integrated ICs to implement a system-on-package (SOP) [12].

The cost factor of such a SOP approach is determined by the cost of the material and the assembly. Many 60 GHz antenna and module implementations have been reported using low-temperature co-fired ceramic (LTCC) material [13]-[14]. However, they are costlier when compared to organic materials, such as liquid crystal polymer. In addition, organic materials can be fabricated using the printed-circuit-board (PCB) technique

suitable for high-volume, low-cost implementation. Interconnects (between the chip and the package) constitute a significant portion of the assembly process. There is a clear trade-off between the cost and the performance; e.g., flip-chip interconnects provide higher performance compared to the performance of wirebonds, but at a much higher cost. In addition, flip-chip interconnects needs a special design of the board. Hence, for low-cost consumer applications, wirebonding provides a better solution provided its lack of performance can be compensated in the system. Such a low-cost organic package with a standard wirebonding technique would help a seamless integration of the package developed for the 60 GHz system. Figure 2.3 shows the photograph of such a low-cost integrated package, where the size is comparable to that of one-cent coin.

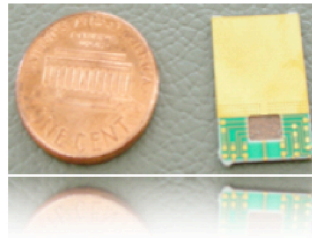


Figure 2.3. Photograph of the integrated 60 GHz module and one-cent coin.

2.3 System architecture and frequency planning

The thesis concentrates on the development of the 60 GHz receiver-front-end building blocks, and eventually the complete receiver front-end. This sub-chapter describes the different receiver front-end architectures, and attempts to evaluate the suitable options for 60 GHz systems.

2.3.1 Heterodyne architecture for 60 GHz systems

In the heterodyne architecture, the received RF signal band is translated to a lower frequency band by a front-end mixer that acts as a simple analog multiplier [15]. The RF frequency (ω_1) is mixed with an oscillator of frequency (ω_0), where ($\omega_0 = \omega_1 - \omega_2$). Hence, the output of the mixer contains two bands of frequencies around ω_2 and $2\omega_1 - \omega_2$. The bandpass filter removes the higher frequency band ($2\omega_1 - \omega_2$), and the frequency ω_2 is defined as *intermediate frequency* (IF). The downconversion mixer is preceded by a low-noise amplifier (LNA) to reduce the noise figure of the system. In case of a 60 GHz system, the RF frequency ω_1 is 60 GHz (specifically 57-64 GHz frequency band). Figure 2.4 shows the basic block diagram of a heterodyne receiver.

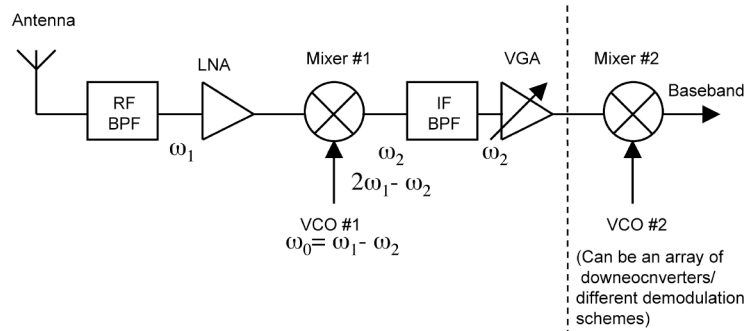


Figure 2.4. Block diagram of a heterodyne receiver.

The frequency planning would depend on multiple aspects in heterodyne architecture; e.g., image frequency rejection and IF bandwidth. The image frequency is the frequency received by the antenna around $(\omega_1 - 2\omega_2)$. This frequency, when mixed with ω_0 , would produce ω_2 (IF). The image frequency is the undesired received frequency in the receivers, and this frequency would cause interference with the desired RF frequency (60 GHz). The image frequency emissions are more of a concern in transmitters, as they are not allowed to emit any signal in the restricted frequency bands. Also, ideally the RF bandpass filter (BPF) would not be used because of the passband-insertion loss of the filter and the complexity of integration. Hence, the antenna and the LNA (PA in the transmitter) in the receiver would provide the bandpass nature around 60 GHz not to receive signals outside 57-64 GHz band. A simple solution is to choose IF to be high enough so that the bandpass response of the front-end (PA/antenna in transmitter and antenna/LNA in receiver) sufficiently rejects the image frequency; e.g., an IF of 20GHz would cause the image frequency to be approximately 20 GHz, and hence, the bandpass response of the antenna and LNA would cancel the image frequency completely. However, IF circuits, e.g., the variable-gain amplifier, the second downconversion mixer, and the second downconversion VCO, would become more complex with the increase in IF.

Another issue is the IF bandwidth supported by the 60 GHz system. In order to maximize the data rate, the entire license-free bandwidth, i.e., 7 GHz, should be translated into IF. It is desired that the second downconversion stage directly translates IF into baseband to minimize the power consumption and complexity of the system. Hence, the data bandwidth can be 3.5 GHz (IF bandwidth/2) at the most. So, the IF needs to be at

least twice the data bandwidth to prevent the *aliasing* of the demodulated data [16]; i.e., the minimum IF should 7 GHz to utilize the entire license-free bandwidth. In addition, the fractional bandwidth of the IF would be lower with increasing IF as the bandwidth is fixed. A smaller fractional bandwidth is easier to realize in IF circuits when compared to a larger fractional bandwidth. The realization of *low-IF* heterodyne receiver architecture is not meaningful because of these data-demodulation and fractional bandwidth requirements.

2.3.2 Homodyne architecture for 60 GHz systems

The homodyne architecture proposes a direct translation of RF frequency into baseband frequency. This architecture is also called *direct-conversion* or *zero-IF* architecture [15]. In this case, the LO frequency is equal to the carrier frequency. Figure 2.5 shows the basic block diagram of a homodyne receiver.

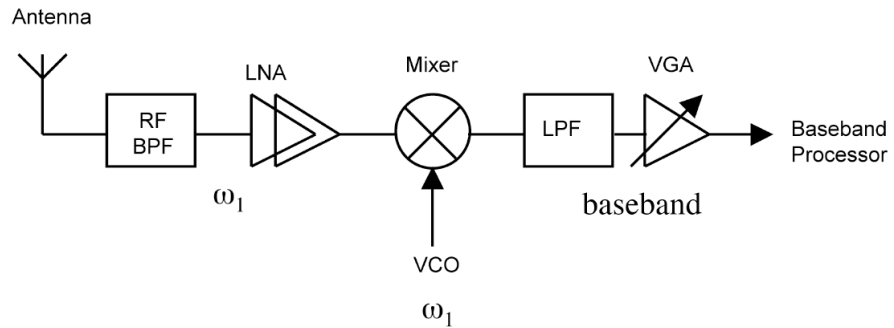


Figure 2.5. Block diagram of a homodyne receiver.

The homodyne receiver has much less components as compared to heterodyne receivers. In addition, the image frequency is circumvented in homodyne receiver because IF is 0. Hence, this homodyne architecture is very simple and suitable for

monolithic integration. However, there are different sets of problems for homodyne architecture.

Firstly, the complexity of the modulation scheme is limited when a direct-conversion architecture is used. Any quadrature modulation scheme, e.g., QPSK and QAM, would require quadrature mixing and quadrature LO generation at 60 GHz. The complexity of a reliable quadrature downconversion is extremely challenging using the available CMOS or SiGe IC processes. The more practical modulation schemes would be ASK, BPSK and minimum-shift keying (MSK). For further simplification, the downconversion scheme may need to be non-coherent for homodyne architectures.

Secondly, since in a homodyne topology, the downconverted band extends to zero frequency, extraneous offset voltages can corrupt the signal, and more importantly saturate the following stages. The DC offset can be generated by the LO leakage, i.e., the LO feedthrough to the RF signal by substrate and capacitive coupling. However, in case of very high data rates (over 1 Gbps), a on-chip series-capacitive coupling (on the order of tens of pF) can still be used in the baseband processor to remove the DC offset before saturation and to demodulate data properly. In addition, *DC-free* modulation schemes and DC offset-cancellation techniques can get rid of the DC-offset issue.

Thirdly, the *even-order distortion* causes the corruption of the downconverted signal of interest. This distortion is reflected in the second-order intermodulation product of the front-end elements. This distortion is more challenging to overcome in case of the complex modulation schemes.

However, the flicker noise issue of the direct-downconversion receivers should not affect the 60 GHz receivers, because the data rate is much higher than the flicker corner

frequency of the downconversion mixer [15]. With the background of both the homodyne and heterodyne receiver architectures, the 60 GHz receiver architectural options are analyzed and evaluated in the next subsection.

2.3.3 60 GHz receiver architecture

As seen in the previous sub-section, the direct-conversion architecture is more suitable for a simple, low-power receiver implementation. However, they are limited in terms of modulation schemes that can be used in 60 GHz multi-Gbps-data-rate system. A more complex heterodyne receiver would be necessary for a high-performance, robust 60 GHz receiver implementation.

Another important aspect of the receiver front-end is the multi-channel implementation. The large available bandwidth (7 GHz) can be divided into multiple channels to facilitate baseband-processing requirements; e.g., low-speed, low-power analog-to-digital converters (ADCs) and low-power data processors. Hence, the architecture should be able to address multi-channel interference issues and channel-bonding (bonding of multiple adjacent channels) capabilities. Both homodyne and heterodyne architectures can minimize adjacent channel interference by using sharp lowpass filters in direct-conversion architecture and sharp IF bandpass filters in heterodyne architecture. In both cases, the VCO#1 frequency can be tuned in order to lock to a particular channel. However, the homodyne architecture is not suitable for channel bonding as the implementation of the tunable lowpass filter is much more difficult compared to the implementation of the tunable bandpass filter.

Table 2.1 summarizes the comparison of performance specifications of different building blocks used in the heterodyne and direct-conversion architectures.

Table 2.1. Comparison of building blocks for different system architectures.		
Building block	Direct-conversion	Heterodyne
LNA	High gain and low noise figure	Medium gain and low noise figure (because additional gain stages are present)
Mixer#1	Wideband double side band (DSB). Minimum LO leakage necessary to minimize DC offset. Hence, passive subharmonic mixing can be a solution.	Wideband single side band (SSB). It need not be quadrature even if data is quadrature.
VGA	DC-broadband. Can be distributed or very high frequency operational amplifier. DC offset compensation required.	Broadband IF variable gain amplifier
Mixer#2	-	Can be an array of mixers with varying frequency local oscillators.
ADC	Requires >5 Gsps sampling rate. Hence, very high power dissipation.	Comparatively lower power dissipation for a multi-channel architecture.

The modulation scheme has to be chosen considering the trade-off between the bit rate and complexity of the hardware. The simplest coherent modulation scheme is BPSK that can provide a bit rate of 3.5 Gbps (upto 5 Gbps with baseband filtering), if the entire bandwidth is utilized. QPSK can double the bit rate, but QPSK requires quadrature mixers and higher sensitivity of the receiver front-end. QAM can double the bit rate as compared to QPSK, but QAM requires a stringent linear operation of the front-end. Frequency-shift keying (FSK) or Gaussian-minimum-shift keying (GMSK) is another relatively simple modulation scheme that can be utilized in a 60 GHz system. The most important aspect of a given modulation scheme is the signal-to-noise ratio (SNR) necessary for a receiver to achieve a specified level of reliability in terms of bit-error rate (BER). A raw BER (before error correction) of 10^{-5} is typically desirable for wireless communications schemes. A graph of E_s/N_0 vs BER is shown in Figure 2.6. E_s/N_0 is the

measure of the required energy per bit relative to the noise power, and E_s/N_0 can be defined as the signal-to-noise ratio (SNR) of the modulation scheme.

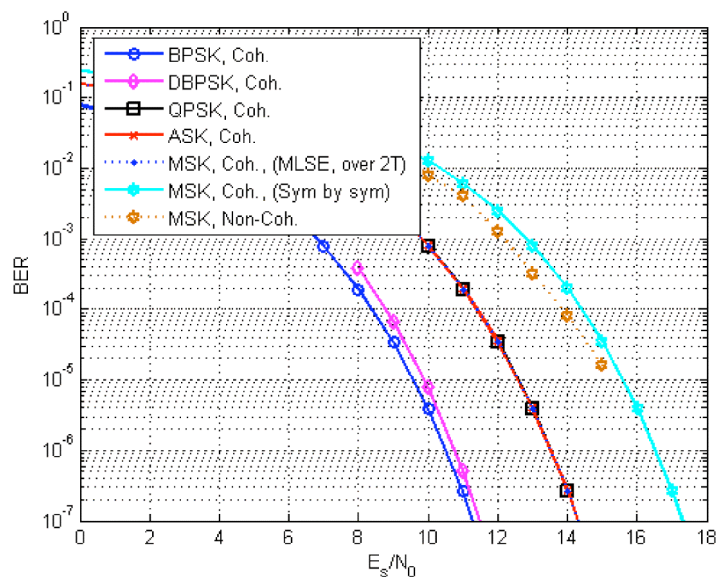


Figure 2.6. Probability of bit error for common modulation schemes.

As seen in Figure 2.6, coherent BPSK is the best solution in terms of the lowest SNR requirement for the same BER. QPSK and coherent ASK require a 3dB higher SNR. However, MSK requires even higher SNR for the same BER requirement.

Amplitude modulation has been explored up to 1.5 Gb/s data rate for video applications [17]. ASK is the simplest architecture, but it is limited by the capacity and SNR. A direct-conversion scheme with QPSK modulation is investigated in [18] with the entire bandwidth of the license-free band. However, the high noise figure (12.5 dB) would not be favorable for a QPSK scheme as shown in the next subsection. A similar scheme is implemented in [19] for 700 Mb/s QPSK data transmission.

2.3.3.1 60 GHz front-end low-noise amplifier

The front-end low-noise amplifier development at 60 GHz is much different as compared to the low-noise amplifier development at lower RF frequencies (2.4/5.8 GHz). At lower RF frequencies, the noise figure of the amplifier is mostly dependent on the noise matching at the input [15], because the minimum noise figure (NF_{MIN}) of transistors are less than 0.5 dB in state-of-the-art CMOS and SiGe IC processes. However, at 60 GHz the minimum noise figure of the transistors is at least 3 dB [20] as reported in the highest performance 0.12 μm SiGe process. The minimum noise figures of 90 nm or 130 nm CMOS processes are even higher compared to the noise figure of 0.12 μm SiGe. In addition, the minimum noise figure constitutes the most significant part of the total noise figure of the amplifier. Hence, the 60 GHz low-noise amplifiers are typically designed with a 50-ohm input power matching instead of a noise matching. Also, the difference in noise figure between the optimum noise matching and power matching can be made less than 1 dB. This difference in noise figure is acceptable as it is much lower than the minimum noise figure of the transistors. The size of transistors and the DC current density are adjusted to realize the minimum noise figure under the maximum power-gain condition [10], [20]-[25].

The input noise-matching and power-matching conditions are simultaneously achieved by using source-degeneration inductors and input series inductor as seen in Figure 2.7 (a). The output-matching network also consists of a spiral inductor. However at 60 GHz, transmission lines have a higher quality factor than spiral inductors [10], and the length of the transmission lines are short enough to realize a compact integration. Figure 2.7 (b) shows a typical 60 GHz LNA implementation in a CMOS process.

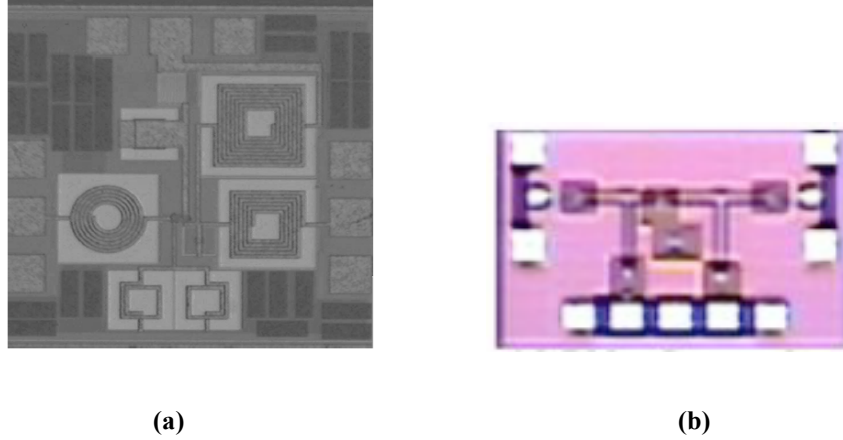


Figure 2.7. (a) Die photograph of a 5 GHz CMOS LNA; (b) Die photograph of a 60 GHz CMOS LNA.

2.3.3.2 60 GHz front-end downconversion scheme

The front-end downconversion mixer can be direct-conversion or heterodyne depending on the system architecture. The input of the mixer is connected to the output of the LNA. The LNA output is usually single-ended. Hence, mostly the reported mixers are not of double-balanced type [18], [26]; i.e., the mixer output contains local oscillator leakage. However, in the higher-end IC processes, active balun is used to generate differential 60 GHz signal, and a double-balanced architecture is realized [20].

The implementation of 60 GHz voltage-controlled oscillators (a little lower frequency for heterodyne architecture) and phase-locked loops is extremely challenging. Hence, subharmonic mixing [27]-[29] is sometimes utilized in the front-end downconversion mixer. In the case of subharmonic mixing, the LO frequency is a sub-multiple of 60 GHz (one-half for 2X mixing, one-fourth for 4X mixing). The passive subharmonic mixers are extremely broadband [28] and suitable for 60 GHz systems. However, a higher LO power requirement and conversion loss are the negative aspects of a subharmonic mixer. The

conversion loss is required to be compensated by a high-gain front-end low-noise amplifier.

The non-coherent direct-downconversion schemes can also be used for amplitude-modulated systems. The advantage of the non-coherent system is the absence of voltage-controlled oscillator and phase-locked loop. Hence, an extremely low-power implementation of the system is possible [30].

2.3.4 Link budget of 60 GHz systems

The sensitivity, dynamic range, gain, noise figure, linearity, and unwanted emissions are the important specifications of a communication system front-end. These specifications are closely related to the overall link budget of the system. According to Friss transmission formula,

$$R = N \sqrt{\frac{P_T G_T \lambda^2}{P_R F_M 16\pi^2}} \quad (2.1)$$

where: R = Maximum range for communication link;

N = Propagation law (N = 2 for line of sight, N = 4 urban environments);

P_T = Transmit power;

G_T = Total antenna gain;

λ = Wavelength;

P_R = Receiver sensitivity;

F_M = Fading margin.

To simplify the equation, a 6 dB higher transmit power, 6 dB higher antenna gain or 6 dB better receiver sensitivity would double the range for line-of-sight links. However,

there are regulatory emission limits on the transmitter power output. Hence, the transmit power cannot be increased in an unrestricted fashion. Figure 2.8 shows the worldwide regulatory limits for the 60 GHz communication schemes.

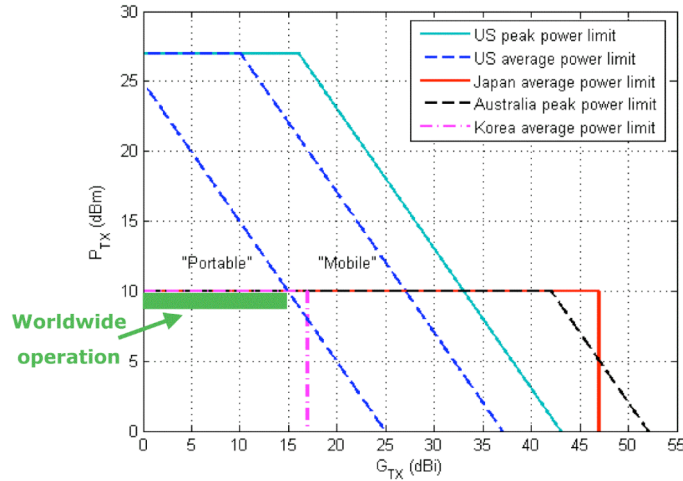


Figure 2.8. Worldwide regulatory transmit power limits for 60 GHz communication.

The antenna gain is also an important factor. In the traditional point-to-point communication schemes, large antennas are used to provide a much higher antenna gain (e.g., 40 dBi-gain horn antennas). However, small form-factor printed antennas need to be used for integrated portable systems. Their typical gain is in the order of 5-15 dBi, and the coverage angle is usually a trade-off factor with antenna gain [31]. To increase the coverage and to have a large gain, antenna arrays need to be used [32]. However, antenna array or phased array also increases the system complexity.

The receiver sensitivity is defined as the weakest signal the receiver can detect. The sensitivity is related to the SNR of the input signal that the receiver would be able to detect. The following equation computes the input noise power to receiver:

$$S = 10\log(KT) + 10\log(B) + NF(dB) + LM(dB) + \frac{E_b}{N_0}(dB) \quad (2.2)$$

where: S = Receiver sensitivity;

$10\log(KT) = -174$ dBm (thermal noise floor);

B = RF bandwidth;

NF = Noise figure of the receiver;

LM = Link margin;

E_b/N_0 = SNR per bit required for proper demodulation.

For BPSK/QPSK modulation schemes, the SNR required for proper demodulation is approximately 9.6 dB for a BER of 10^{-5} . The noise figure of the receiver (LNA, front-end mixer, and IF stages combined) can be taken as approximately 10 dB. Hence, for a RF bandwidth of 2 GHz and zero link margin, the sensitivity is computed as -61 dBm. Typically 6 dB of link margin for a proper operation would worsen the sensitivity to -55 dBm. For complex modulation schemes, a higher SNR would be required, and thus, the sensitivity would be worsened.

The receiver-sensitivity figure is important in two aspects; firstly, it is critical that the receiver architecture can work with the receiver-sensitivity figure (i.e., a proper demodulation can be performed), and secondly, the receiver-sensitivity figure should correspond to a reasonable link distance. The first aspect can be taken care of by a suitable receiver architecture and an efficient design of building blocks. The second aspect is related to the equation 2.2, and this aspect is critical for the link distance, i.e., the distance between the transmitter and the receiver. It is easier to satisfy the first condition; i.e., to develop a suitable receiver architecture. But the SNR requirement for

the proper baseband demodulation limits the receiver sensitivity; e.g., -55dBm for the previous example.

Figure 2.9(a) shows a plot between the link distance and the data rate (assuming 2 GHz RF bandwidth is required per Gbps of uncoded data rate assuming BPSK modulation scheme) for line-of-sight 60 GHz wireless links for different link margins. The antenna gain is assumed to be 10 dBi for both transmitter and receiver. The transmit power is assumed to be 5 dBm as a reasonable estimate for CMOS power amplifiers at 60 GHz [22]. The data rate would determine the required RF bandwidth, and the RF bandwidth would determine the sensitivity of the receiver. The similar plot is drawn in Figure 2.9(b) for a 10 dBm output power (multiple parallel power-amplifier stages) and 15 dBi antenna gain (phased array systems).

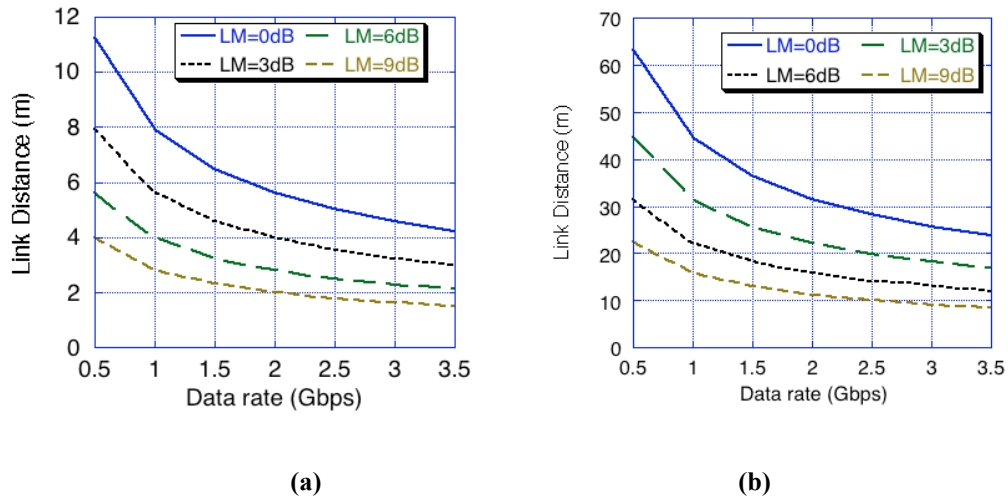


Figure 2.9. (a) Wireless-link distance vs. uncoded data rate for a single-antenna low-power 60 GHz communication scheme. (b) Wireless-link distance vs. uncoded data rate for a phased array 60 GHz communication scheme.

Approximately 2-5 m of wireless link distance can be achieved with different link margins as shown in Figure 2.9(a). However, the link distance of greater than 10 m can be easily achieved with phased array systems. The later link can also be non-line-of-sight

(NLOS) because of a large link margin at shorter distances. Spectrally efficient modulation schemes can increase the data rate for the similar link distance and link margins; i.e., the data rate with QPSK modulation would be twice the data rate with BPSK modulation, and the data rate with QAM modulation would be twice the data rate with QPSK modulation. However, the complexity of the receiver architecture and building blocks increase with the increase in the spectral efficiency of the modulation schemes. On the other hand, filtering and pulse shaping can increase the data rate for similar link distance and link margins. However, the baseband filtering and pulse shaping also demands stringent linearity specifications from transceiver building blocks.

2.4 **Hybrid integration approach**

In this subsection, a proof-of-concept system-integration approach has been demonstrated for multi-gigabit modulation/demodulation at 60 GHz. This intermediate integration approach is different from traditional stand-alone component-based millimeter-wave integration approach. This intermediate approach is suitable for small form-factor integration. A passive subharmonic anti-parallel-diode-pair-based (APDP-based) mixing [33] scheme has been selected as the demonstration of hybrid integration scheme. The term *hybrid* refers to a heterogeneous integration between the IC and package. This integration consists of stand-alone ICs and transmission lines on the package substrate. The hybrid integration is lower cost and more compact compared to the cost and size of the traditional stand-alone-component-based millimeter-wave modules. Low-noise amplifiers and power amplifiers are active components, and their performance depends mostly on the performance of transistors. Hence, they are more suitable to monolithic integration compared to hybrid integration. On the other hand, the performance of the passive mixer is dependent on the IC process and matching networks consisting of transmission lines. An APDP-based subharmonic mixer is inherently direct-conversion in nature. However, the design can be modified for superheterodyne architectures. Hence, a passive mixer has been chosen as the demonstration for hybrid integration.

2.4.1 Subharmonic-mixer conversion-loss characterization

Traditionally diode mixing is popular in millimeter-wave domain using high performance Schottky barrier diodes as mixing components. Figure 2.10 shows an equivalent circuit diagram of a diode for large-signal and small-signal scenarios. C_j , C_{j0} , R_j and R_s defines the junction capacitance, zero-bias junction capacitance, junction resistance, and extrinsic series resistance (channel and contact resistance combined), respectively.

The cut-off frequency of the diode is given by

$$f_c = \frac{1}{2\pi R_s C_{j0}} \quad (2.3)$$

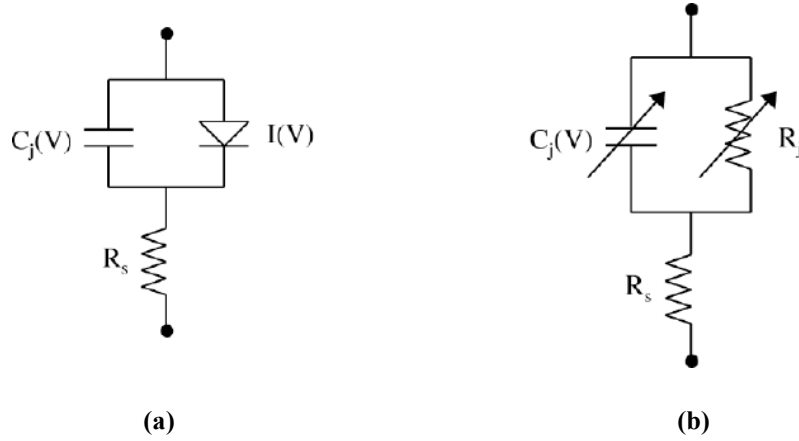


Figure 2.10. (a) Diode large-signal equivalent circuit; (b) Diode small-signal equivalent circuit.

It is obvious that reducing the series resistance and zero-bias junction capacitance would increase the operating frequency of circuits. Hence, small-area Schottky diodes are suitable for high-frequency circuits. Figure 2.11 shows the APDP-mixing-core topology and the operation of the mixer.

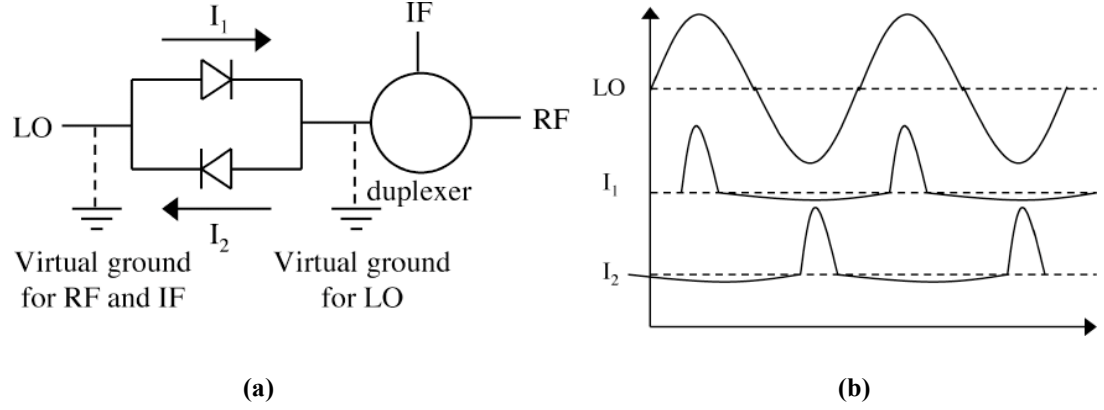


Figure 2.11. (a) Schematic of the APDP core; (b) LO signal and current through the mixing diodes.

The LO voltage can be considered as much higher compared to RF and IF voltages and the instantaneous currents through the diodes are given by

$$I_1 = I_s(e^{\alpha V_{LO}} - 1) \quad (2.4)$$

$$I_2 = -I_s(e^{-\alpha V_{LO}} - 1) \quad (2.5)$$

Here, I_s is the reverse saturation current of the diodes, and α is the diode-slope parameter. The transconductance of each of the diodes is given by

$$g_1 = \frac{\partial I_1}{\partial V} = \alpha I_s e^{\alpha V_{LO}} \quad (2.6)$$

$$g_2 = \frac{\partial I_2}{\partial V} = \alpha I_s e^{-\alpha V_{LO}} \quad (2.7)$$

The overall transconductance of the APDP core is given by the sum of individual transconductances of two diodes (at least one of the diodes is active during one-half cycle of the LO) as shown below:

$$g = g_1 + g_2 = 2\alpha I_s \cosh(\alpha V_{LO}) \quad (2.8)$$

The mixing output contains only even harmonic mixing terms as predicted by the nature of “Cosh” function. The conversion loss depends on the characteristics of the

diode and the LO voltage (before saturation). The slope parameters of the GaAs diodes are usually higher than that of the silicon diodes.

2.4.2 Development of 4X mixer on liquid crystal polymer

A stand-alone Agilent HSCH9251 GaAs beam-lead Schottky-barrier APDP chip is used for the generation of non-linearity. Different passive elements are fabricated on LCP, and the APDP package is soldered on LCP. Two different versions are implemented at 40 GHz and 60 GHz [28].

2.4.2.1 40/60 GHz passive development on LCP

A planar bandpass filter architecture with microstrip transmission lines (bottom-ground plane distance = 100 μm) has been chosen for the ease of integration and to minimize the cost. The bandwidth of the bandpass filter would determine the maximum data rate in a direct-conversion architecture. Hence, in order to utilize the entire license-free bandwidth, 10% fractional-bandwidth specifications are targeted. However, the design-rule specifications (minimum line width and spacing = 75 μm) restrict the design of coupled sections. A larger ground-plane distance would help the design, but that would increase the radiation loss in the microstrip configuration. A 3rd order coupled line filter, designed in low impedance environment (25 Ω), satisfies the design rules, while the fractional bandwidth is increased to approximately 14 % [34]. Quarter-wavelength transformers transform the impedance to 50 Ω at input and output ports of the filter. The design has been tuned using EM simulators to account for variations as a result of thick-metal and dispersion effects at millimeter-wave frequencies. A 40 GHz version has also been implemented to verify the design methodology.

The 60 GHz bandpass filter occupies an area of 4 mm×1.22 mm on LCP substrate. It has been measured using Agilent 8510XF vector network analyzer (2-110 GHz) and Cascade Microtech 250 μ m pitch air coplanar probes. The measurement results show approximately 3 dB insertion loss with 8 GHz 3-dB bandwidth. The 40 GHz filter has been measured using Agilent 8510C vector network analyzer. The measurement results show 3 dB insertion loss with 6 GHz 3-dB bandwidth. A slight variation (\sim 2-3%) of the center frequency can be attributed to the dielectric thickness variation and overestimation of the dielectric constant of LCP during simulation. The corrected simulation results and the measurement results have been shown in Figure 2.12(a) and Figure 2.12(b).

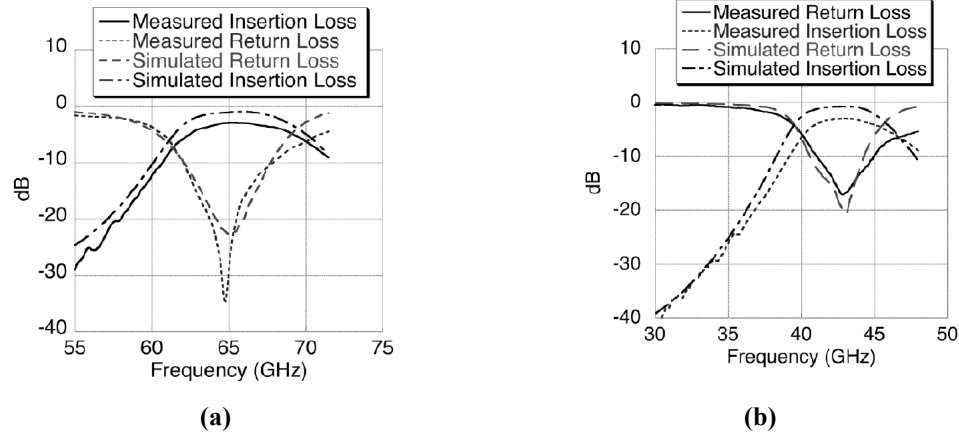


Figure 2.12. (a) 60GHz bandpass filter performance; (b) 40GHz bandpass filter performance.

This filter is utilized in the development of a novel RF/baseband duplexer that is a building block of the 4X subharmonic mixer. It combines RF and baseband signals in the direct-conversion scheme, and carries them to the APDP for mixing. Specifications of the duplexer include the necessary rejection at the 1st, 2nd, and 3rd harmonic of the 15 GHz LO frequency; i.e., at 15 GHz, 30 GHz, and 45 GHz to suppress even-order mixing terms and the odd-order LO harmonics generated by APDP [35]. The $\lambda_g/4$ open stubs at

different frequencies provide the necessary rejection. The duplexer occupies only 4 mm × 2.5 mm area on LCP substrate. A 40 GHz version of the duplexer has also been fabricated for characterization. Figure 2.13(a) shows the function and structure of the duplexer. Figure 2.13(b) and Figure 2.13(c) show the photos of fabricated filters and duplexers.

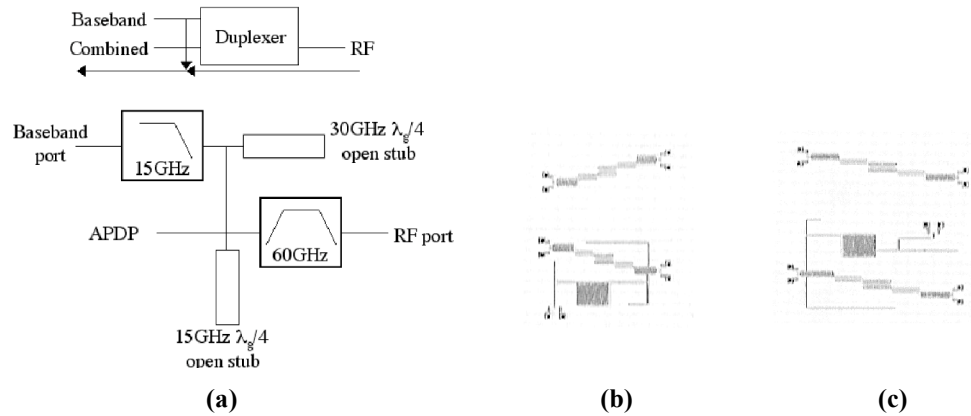


Figure 2.13. (a) 60 GHz duplexer architecture; (b) Fabricated 60 GHz filter and duplexer; (c) Fabricated 40 GHz filter and duplexer.

The 60 GHz duplexer shows 3.5 dB measured insertion loss in RF path with 6.5 GHz 3-dB RF bandwidth. The low pass section is measured to have 12 GHz 3-dB bandwidth with approximately 25.5 dB rejection at 15 GHz. The measurement results of the 40 GHz duplexer indicate 3 dB insertion loss in RF path with approximately 30 dB isolation between RF and baseband ports. The spurious response from the low pass section is measured to be less than 35 dB in the entire passband. Measurement results and simulation results are compared in Figures 2.14(a), 2.14(b), and 2.14(c).

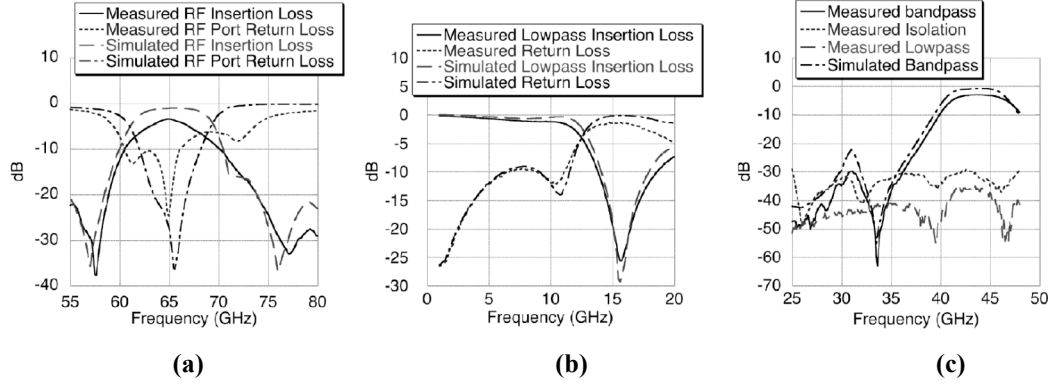


Figure 2.14. (a) Bandpass performance of 60 GHz duplexer; (b) Lowpass performance of 60 GHz duplexer; (c) Bandpass performance of 40 GHz duplexer.

2.4.2.2 4X subharmonic mixer development on LCP

The EM-simulated s-parameter data of passive elements are combined with the APDP model in Agilent ADS simulator to perform the complete simulation of the 4X subharmonic mixer. The mixer can be used for both down and up conversion. Agilent HSCH9251 GaAs beam-lead Schottky barrier APDP is integrated with various passive elements on LCP. Table 2.2 shows different diode parameters.

Table 2.2. Agilent HSCH9251 diode parameters.	
Diode Properties	Value
Saturation current (pA)	0.16
Series resistance (Ω)	5
Emission coefficient	1.2
Junction capacitance (pF)	0.04
Built-in voltage (V)	0.7
Bandgap voltage (eV)	1.43
Reverse breakdown voltage (V)	5
Breakdown current (uA)	100

The 30 GHz $\lambda_g/4$ open stub in the duplexer suppresses $(f_{RF}-2f_{LO})$ and $(6f_{LO}-f_{RF})$ mixing component. The 15 GHz and 45 GHz $\lambda_g/4$ open stubs suppress f_{LO} and $3f_{LO}$ components. Hence, only $(f_{RF}-4f_{LO})$ component is transmitted to the baseband port. The 60 GHz $\lambda_g/2$ short stub provides a short circuit for both RF and baseband signals. Hence, the entire RF signal is available across the diode pair to reduce the conversion loss. In

addition, baseband signal cannot leak through the diode, and load the LO source. This 60 GHz $\lambda_g/2$ short stub provides high impedance at LO frequency. Hence, a negligible LO power leaks through the stub to ground. The RF/baseband port of the diode pair is short at LO (as a result of 15 GHz $\lambda_g/4$ stub in the duplexer). Hence, the entire LO power is available across the diode pair. Using a 60 GHz λ_g short stub instead of $\lambda_g/2$ short stub would present a perfect open for the LO, but the improvement is negligible. Also, the smaller stub occupies less area on the LCP substrate. The schematic of the mixer is shown in Figure 2.15(a). A LO-matching network is required in order to minimize LO-power requirements and the unwanted reflection into the LO source. Usually the diode pair (other end shorted) provides a capacitive impedance to LO signal. The 60 GHz $\lambda_g/2$ short stub transforms the look-in impedance of the diode pair at 15 GHz to approximately 50Ω at 8 dBm power level as shown in Figure 2.15(b). Hence, there is no need of additional matching network at the LO port. Figure 2.15(b) shows the simulated impedance of the APDP (the other end shorted) at LO frequency (15 GHz) at different power levels in the Smith chart for three different cases; i) without any short stub, ii) with λ_g short stub, and iii) with $\lambda_g/2$ short stub.

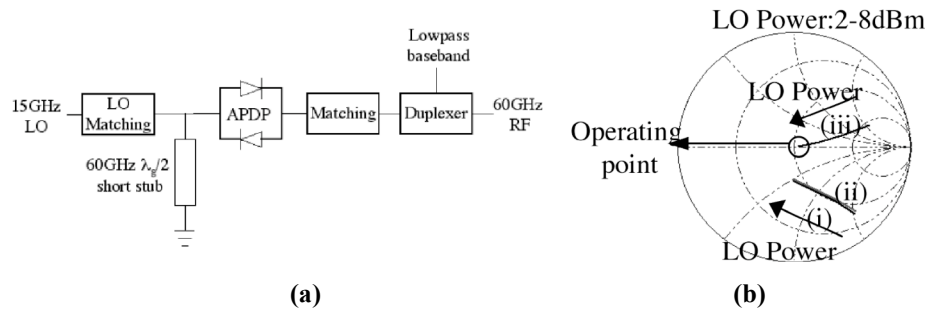


Figure 2.15. (a) Schematic of the 4X mixer; (b) Simulated input impedance of APDP at 15 GHz (other end shorted) at different LO power levels for i) without any stub, ii) with 60 GHz λ_g short stub, and iii) with 60 GHz $\lambda_g/2$ short stub.

For the 40 GHz subharmonic mixer, a separate LO-matching network with an open stub is implemented. Another small interstage-matching network has been placed between the APDP and the duplexer. This interstage-matching network modifies the look-in impedance of the APDP as seen by the duplexer, and optimizes the conversion loss and bandwidth performance of the subharmonic mixer. Care has been taken so that the matching network does not affect LO-matching conditions. Figure 2.16(a) describes the simulated conversion loss of the 60 GHz mixer with and without the LO and interstage matching (optimized or not optimized). Figure 2.16(b) and Figure 2.16(c) show photos of the fabricated 60 GHz and 40 GHz 4X mixers.

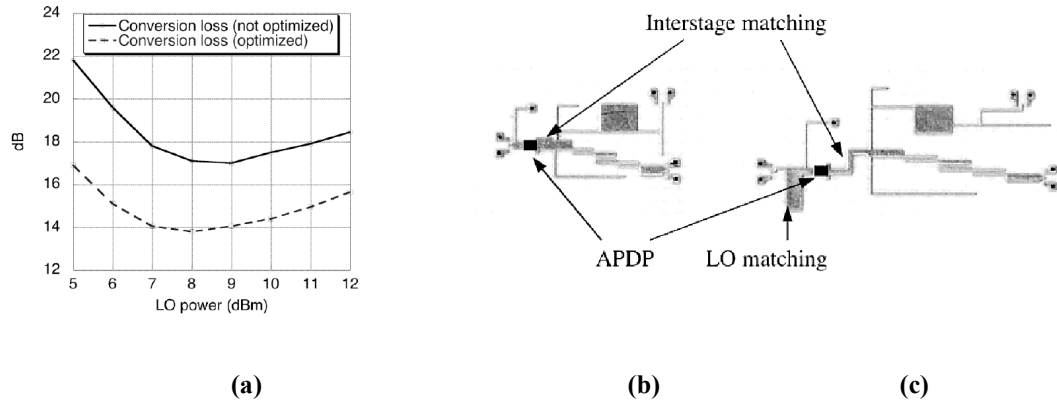


Figure 2.16. (a) Simulated mixer conversion loss before and after optimization; (b) Photo of fabricated 60 GHz 4X mixer; (c) Photo of fabricated 40 GHz 4X mixer.

Here we see approximately 3 dB improvement in the simulated conversion loss using optimization techniques in the interstage-matching network. In addition, the minimum loss occurs at a lower LO power level (8 dBm instead of 9 dBm). The optimized mixer occupies an area of 5.2 mm×2.7 mm on LCP.

The mixer characterization has been performed with a single-tone signal. The frequency and power of baseband signal are varied to obtain the complete conversion loss

and bandwidth performance. Approximately 17 dB conversion loss with a single sided 3-dB bandwidth of 1.25 GHz has been measured at 7.5 dBm LO power and LO frequency of 16 GHz. Measurement results show a 28 dB LO rejection at the RF output. Figure 2.17(a) and Figure 2.17(b) show the variation of the conversion loss with baseband power level (500 MHz single-tone baseband) and baseband frequency (-20 dBm baseband power), respectively. An input 1-dB compression point of -2 dBm is observed. Figure 2.17(c) shows the variation of the conversion loss with respect to LO power using a 500 MHz single-tone -20 dBm baseband signal. Figure 2.17(d) shows the variation of the conversion loss with a varying LO frequency for the same baseband signal at 8 dBm LO power level. The 40 GHz version is measured to have a conversion loss of 16 dB with 1.2 GHz baseband 3-dB bandwidth at 8.5 dBm LO power. The 3 dB difference in the conversion loss between simulation and measurement can be attributed to additional loss of bandpass filters (1.5-2 dB) and interconnect parasitics of the diode pair. The reduction of the bandwidth (around 1 GHz) is also attributed to the mounting of the diodes that affect the metallization on LCP. However, measured results indicate an excellent performance of a stand-alone 4X mixer integrated on LCP.

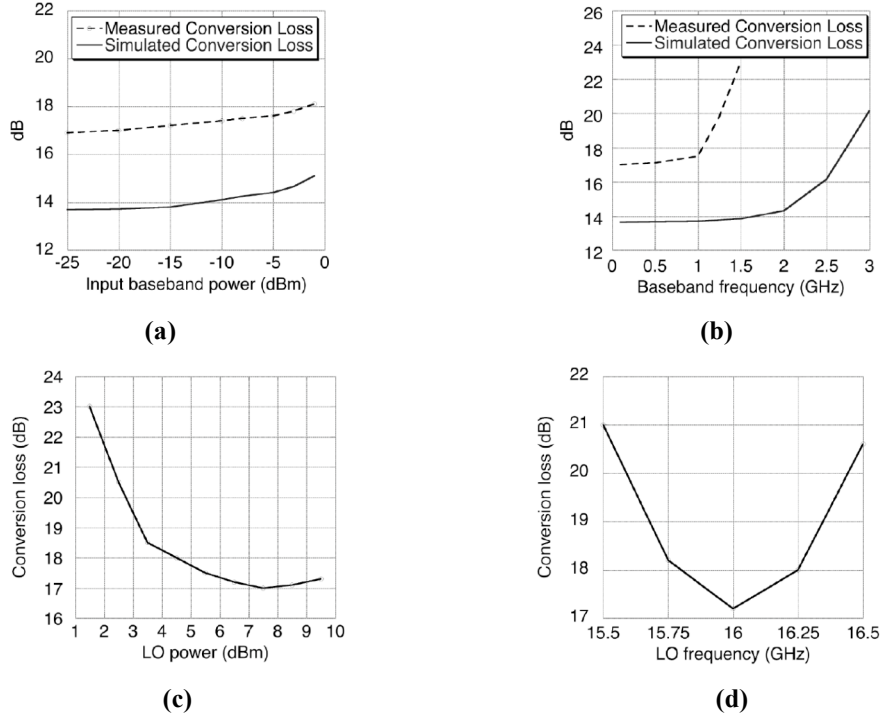


Figure 2.17. (a) Mixer-conversion-loss variation with baseband power level; (b) Mixer-conversion-loss variation with baseband frequency; (c) Measured mixer-conversion-loss variation with LO power level; (d) Measured mixer-conversion-loss variation with LO frequency.

A back-to-back upconversion and downconversion chain is implemented by connecting the RF ports of two identical subharmonic mixers. Typically, it works as a simultaneous BPSK modulator/demodulator when LO phases of the two mixers are synchronized. The measurement setup is shown in Figure 2.18(a). In the downconverter-LO path, a phase shifter is placed for the proper BPSK demodulation. Measurements have been performed for both single-tone baseband and digital PRBS (pseudo-random-binary-sequence). Figure 2.18(b) shows the received spectrum of the simultaneous up and down-converted 500 MHz -10 dBm signal. Figure 2.18(c) shows the received spectrum of 1.5 Gb/s PRBS (500 mV peak-to-peak input followed by a 10 dB attenuator). Figure 2.18(d) shows the received eye diagram for the same input (additional low pass filter

used to attenuate LO leakage). The eye diagram shows an SNR of 13.15 dB in the received signal and a time jitter of 300.3 ps.

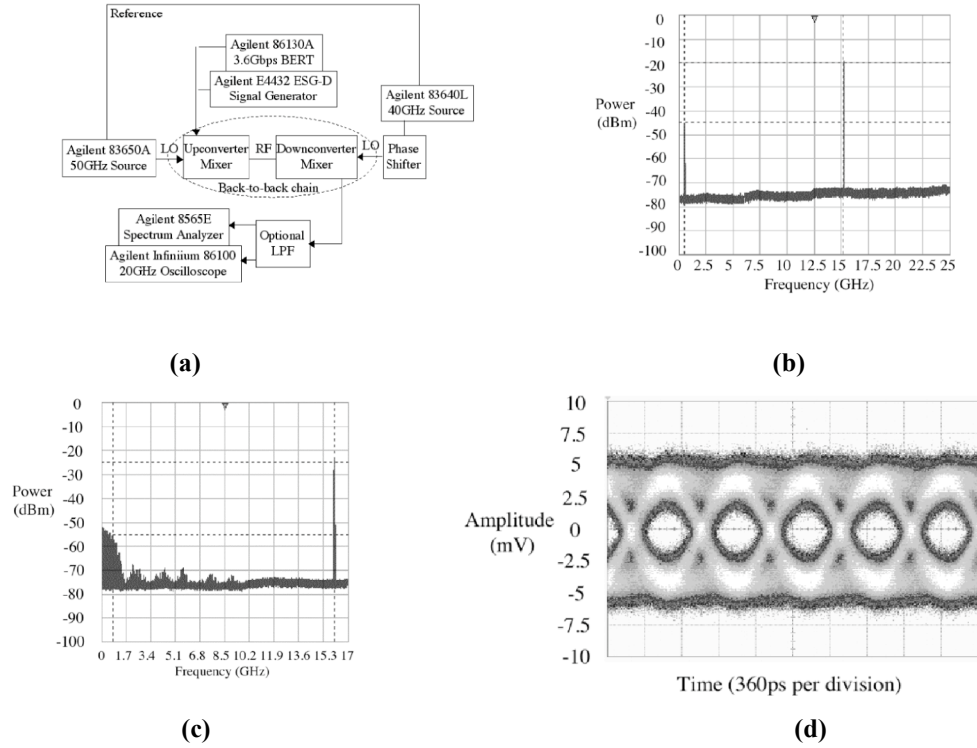


Figure 2.18. (a) Gigabit modulator/demodulator measurement setup; (b) Received single-tone spectrum; (c) Received spectrum of 1.5 Gb/s PRBS (without external LPF); (d) Received eye-diagram of 1.5 Gb/s PRBS (with external LPF).

2.4.3 Hybrid integration summary

The hybrid integration shows decent performance. However, the cost of GaAs diodes is still high and cannot be compensated with low-cost organic module. In addition, the random performance-degrading factors, e.g., soldering of diodes on organic material, additional interconnect parasitic of APDP, large number of 60 GHz wirebonds (from antenna to PA/LNA, from PA/LNA to module, from module to APDP), oppose the realistic large-scale implementation of hybrid integration approach. On the other hand, a monolithic integration on silicon would have advantages in terms of cost, reliability, and

performance. Hence, a silicon-based monolithic integration approach is investigated in subsequent chapters toward a convergent system.

2.5 Summary

In this chapter, an evolution of the millimeter-wave IC and packaging has been presented. A convergent approach is presented toward a low-cost, low-power 60 GHz multi-gigabit system development in terms of front-end silicon-based ICs, module, and signal processing requirements. The homodyne and heterodyne system architectures are described and compared for the realization of 60 GHz systems. A brief summary of receiver front-end building blocks, e.g., low-noise amplifiers and downconversion schemes is presented. In addition, the link budget for a multi-Gbps 60 GHz architecture and the frequency planning are also analyzed. Finally, a hybrid-integration concept is demonstrated using a low-cost organic platform. The hybrid approach acts as the link between the traditional approach and the integrated low-cost approach suitable for a portable 60 GHz system. However, it is shown a monolithic integration on silicon would have advantages in terms of cost, reliability, and performance. Hence, a silicon-based monolithic integration approach is investigated in subsequent chapters toward a convergent system.

Chapter 3

60 GHz Receiver Front-end in SiGe

3.1 Introduction

In this chapter, a low-power architecture for the development of 60 GHz receiver front-end is demonstrated using SiGe process. The direct-conversion architecture is suitable for low-complexity low-power front-end development as shown in this chapter. In order to minimize the cost of the integrated chip, most of the work has been performed in the 0.18 μm SiGe process. Although, this 0.18 μm process has much worse performance compared to the state-of-the-art 0.12 μm SiGe process, the innovative design techniques can compensate for the critical design parameters, and make the cost-performance factor more attractive for 0.18 μm process.

The characterization of passive devices (transmission lines and capacitors) is very critical for 60 GHz designs. Hence, a detailed characterization procedure is described in this chapter. The characterization procedure includes different de-embedding schemes that need to be adopted for different devices.

There are two alternatives for a low-power and low-cost architecture. The first alternative is a non-coherent demodulation to remove the necessity of voltage-controlled oscillators and corresponding synchronization circuits. Amplitude detection is the most simple non-coherent demodulation scheme. The second alternative is a passive

subharmonic mixing approach to reduce the power consumption of the mixing scheme and to reduce the oscillator frequency and power consumption.

In the amplitude detection scheme, the noise figure of the detector is high. Hence, the gain of the front-end amplifier needs to be high to reduce the overall noise figure of the system and improve the sensitivity of the receiver. The subharmonic approach also requires a large gain of the front-end amplifier to compensate for the conversion loss of the mixer. The low-cost implementation demands the use of low-cost IC processes. Hence, the next step is the development of a high-gain and low-noise front-end amplifier using innovative techniques. Such an implementation using a novel gain-boosting technique for millimeter-wave cascode amplifiers is presented in this chapter. A low-power low-noise amplifier is also fabricated in the state-of-the-art process for comparison purpose.

Low-power amplitude detection and passive subharmonic mixing schemes are described using 0.18 μm SiGe process in the subsequent sub-chapters. Both downconversion schemes are suitable for a low-performance IC process without the requirement of 60 GHz oscillators and frequency synthesizers.

After the development of receiver building blocks, their monolithic integration is described. Complete receiver front-ends are developed for the amplitude-detection and passive subharmonic-mixing schemes. These are the first reports of 60 GHz integrated receivers in low-cost 0.18 μm SiGe. In case of the amplitude-detection scheme, the baseband output can be directly connected to 1-bit ADCs or limiting amplifiers for the recovery of data. A low-cost signal-processing technique is sufficient for such a data recovery. The integrated receiver IC is packaged in a low-cost LCP-based organic

module with a printed small form-factor antenna. The non-coherent receiver module provides the complete antenna to demodulated baseband multi-gigabit (up to 2 Gbps) solution for only 25 pJ/bit power budget. This is the *lowest reported* power consumption for any 60 GHz receiver till date. The second monolithic integration in $0.18 \text{ }\mu\text{m}$ SiGe incorporates a passive subharmonic mixer with the front-end high-gain amplifier. A on-chip cross-coupled VCO is also integrated with the front-end. A conversion gain of around 16 dB with a 4 GHz RF bandwidth is demonstrated for a DC power consumption of only 27 mW (62 mW in case of on-chip integrated VCO). This is the first reported subharmonic 60 GHz front-end in $0.18 \text{ }\mu\text{m}$ SiGe.

Finally, the SiGe-based receiver front-end development is summarized, and the possible applications and limitations are discussed in this chapter.

3.2 Characterization of passive elements in SiGe

The characterization of transmission lines and capacitors are essential to design matching networks in millimeter-wave circuits. Transmission lines are microstrip or conductor-backed coplanar waveguide (CB-CPW) to shield the electromagnetic field of transmission lines from the lossy silicon substrate. The top metal layer is typically the thickest layer, and hence, the top metal layer is used as the signal line to minimize resistive losses. The bottom metal layer or some intermediate thin metal layer can provide the bottom ground shield. In most of SiGe processes, the bottom ground layer is meshed in it to satisfy the metal density requirements. However, the hole in the ground plane should be rectangular in shape, and along the length of the transmission line to reduce the field loss through the hole. Two-port s-parameter measurements of the transmission lines and capacitors provide the full passive characterization. Measurements need to be properly de-embedded to appropriate reference planes.

The reference planes move to the tip of the probe with a proper calibration of the vector network analyzer (VNA). However, the on-wafer test structure would have feeding bondpads that need to be properly deembedded. Figure 3.1 shows a block-diagram of the calibration and deembedding reference planes.

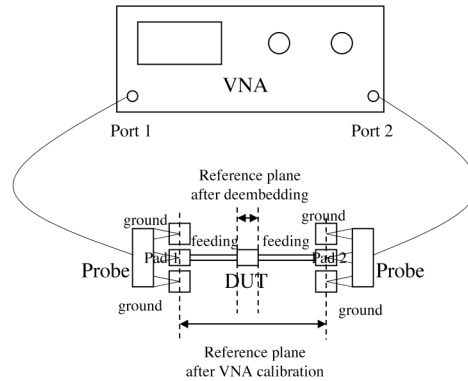


Figure 3.1. Calibration and deembedding reference planes in s-parameter measurement.

An open-short deembedding scheme is used up to 20 GHz. The Y-parameter of the open is subtracted from the measured DUT Y-parameter, and the Z-parameter of the short is subtracted from the measured DUT Z-parameters. The Y-parameter subtraction deembeds the capacitive effect of the bondpad, and the Z-parameter subtraction deembeds the inductive effect of the feeding transmission lines. The lumped-element estimation of the bondpad and feeding transmission line is only accurate up to 20 GHz [37], and hence the open/short deembedding scheme is not accurate over 20 GHz due to the distributed nature of the bondpad and feeding structures.

There are three different alternatives investigated for a proper two-port deembedding of the test structures at 60 GHz. The first one is the *thru* deembedding. The *thru* structure is defined as the structures when two bondpads (with feeding line) are directly connected side by side. A typical *thru* structure is shown in Figure 3.2 (a). Figure 3.2(b) shows the die photograph of a typical DUT (a 60 GHz quarter-wave resonator). The *half-thru* in Figure 3.2 is defined as one-half of the *thru* structure. Two-port s-parameters of both *thru* and DUT are measured. Both S-parameters are converted into corresponding ABCD parameters [38]. If A_T is the measured ABCD parameters of the *thru*, A_D is the measured ABCD parameters of the raw DUT, A_d is the computed ABCD parameters of the deembedded DUT, and A_t is the computed ABCD parameter of *half-thru*, then

$$[A_t].[A_t] = [A_T] \quad (3.1)$$

$$[A_t].[A_d].[A_t] = [A_D] \quad (3.2)$$

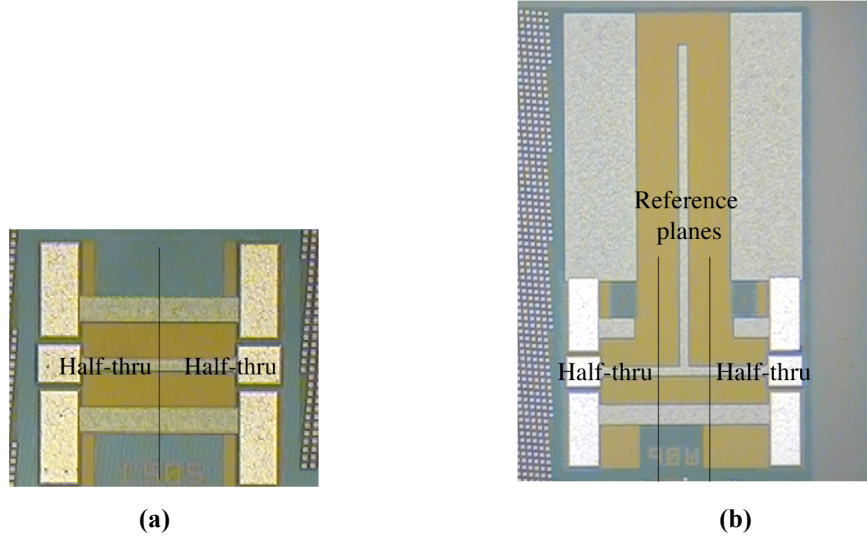


Figure 3.2. (a) Die photograph of the *thru* deembedding structure; (b) Die photograph of the corresponding DUT.

The second alternative for a proper deembedding is the conventional on-wafer *thru-reflect-line* (TRL) calibration [39]. An on-wafer reflection structure (usually open), a *thru* structure, and one or multiple *line* structures are used for this calibration process. The third alternative is the on-wafer line-reflect-match (LRM) calibration [40]. The short structure is not very useful for the implementation of reflect structure because of the ground resistance and inductance. Hence, an open structure, a *thru* structure, and a broadband load structure (port-to-ground 50Ω resistor). The port-extension feature of the VNA is used to subtract the phase of the *thru* structure.

The three different deembedding schemes are compared for different transmission line and passive test structures; (a) 1 mm long 50Ω microstrip transmission line, (b) 60 GHz quarter-wave resonator, and (c) 60 GHz quarter-wavelength coupled line. Die photographs of these test structures, fabricated using $0.15\mu\text{m}$ SiGe process, are shown in Figure 3.3. Figures 3.4(a), 3.4(b), and 3.4(c) show the deembedded performance of the microstrip line, resonator, and coupled line respectively. Figure 3.5(a) shows the die

photograph of the fabricated 200 fF metal-insulator-metal (MIM) capacitor in 0.15 μm SiGe process. Figure 3.5(b) shows the deembedded capacitance value of the fabricated MIM capacitor. Figure 3.6(a) shows the die photograph of 600 μm CB-CPW transmission line in 0.18 μm SiGe process, and Figure 3.6(b) shows the deembedded s-parameters. The similar structures are characterized in different SiGe processes of interest.

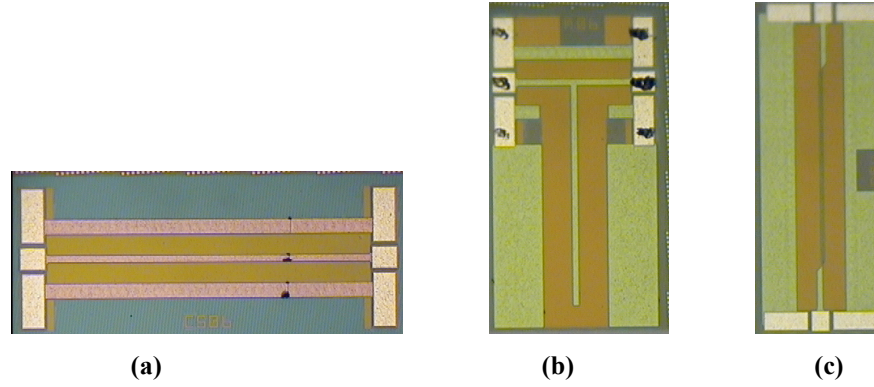
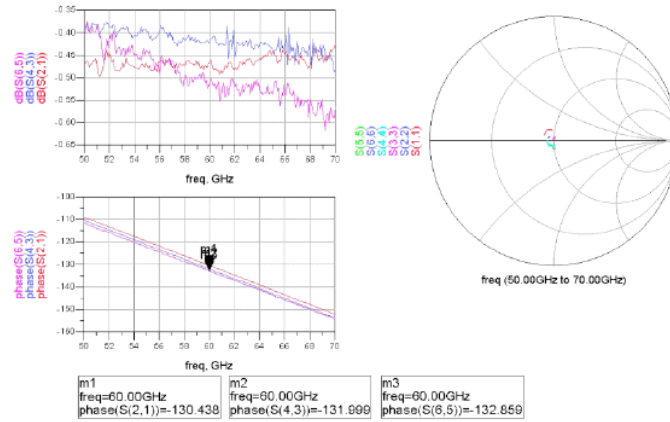
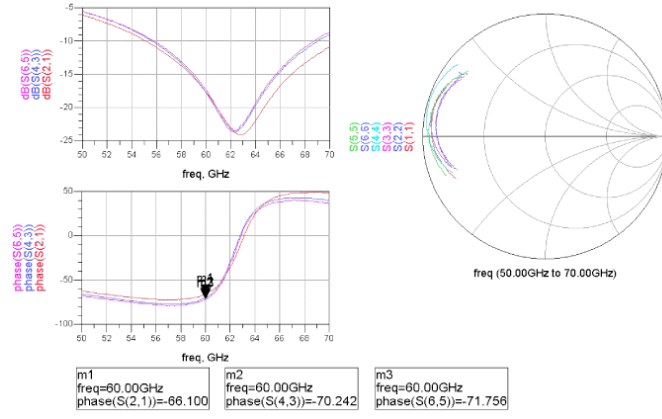


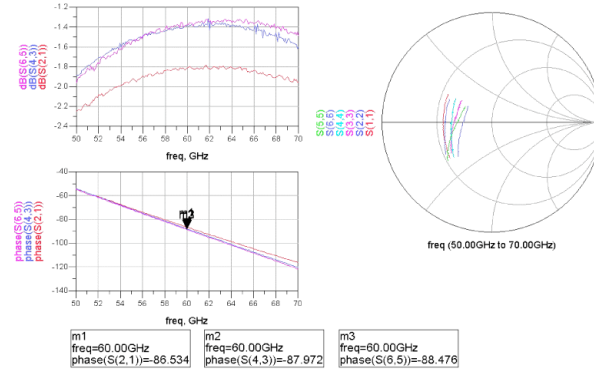
Figure 3.3. (a) 1 mm long 50 Ω microstrip transmission line; (b) 60 GHz quarter-wave resonator; (c) 60 GHz quarter-wavelength coupled line (width = 5 μm , spacing = 4 μm).



(a)

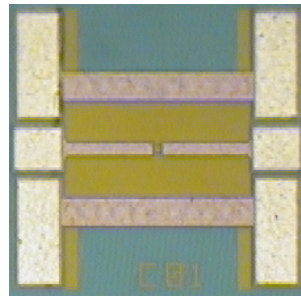


(b)

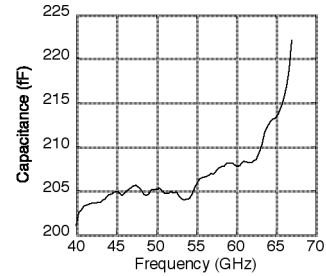


(c)

Figure 3.4. (a) Characteristics of a 1 mm long $50\ \Omega$ microstrip transmission line; (b) Characteristics of a 60 GHz quarter-wave resonator; (c) Characteristics of a 60 GHz quarter-wavelength coupled line (width = $5\ \mu\text{m}$, spacing = $4\ \mu\text{m}$) [Port 1/2 corresponds to standard ISS calibration and ABCD deembedding, port 3/4 corresponds to on-wafer TRL calibration, port 5/6 corresponds to on-wafer LRM calibration].

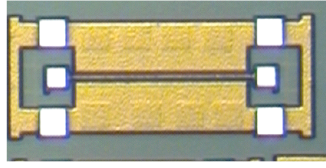


(a)

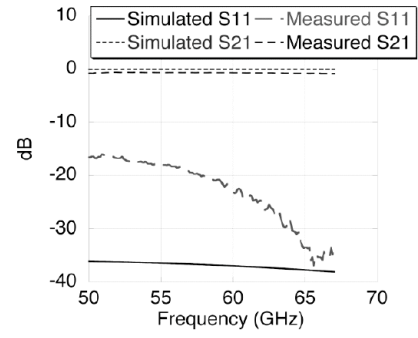


(b)

Figure 3.5. (a) Die photograph of a 200 fF MIM capacitor; (b) Deembedded capacitance of the 200 fF MIM capacitor with frequency.



(a)



(b)

Figure 3.6. (a) Die photograph of a 600 μm CB-CPW transmission line in 0.18 μm SiGe; (b) Deembedded s-parameters of the 600 μm CB-CPW transmission line in 0.18 μm SiGe.

3.3 Low-power 60 GHz front-end LNA development

As mentioned in the second chapter, the gain of the front-end amplifier is required to be high for the direct down-conversion architecture to ensure a good receiver sensitivity (so that the noise figure of the subsequent stages do not impact the overall receiver noise figure and sensitivity). In addition, a low-power implementation is necessary to fit the low-cost, low-power, and low-complexity direct down-conversion specifications. There are two alternatives to realize a low-power and high-gain LNA. The first alternative is to use the high-performance state-of-the-art IC process [19]-[20]. The second alternative is to develop innovative gain-boosting technique using lower-end IC processes. The second alternative is much more attractive in terms of the cost factor, but is more challenging and difficult to implement. In this chapter, three-stage gain-boosted low-power 60 GHz front-end LNA, developed using 0.18 μm SiGe process, is investigated and implemented. The first alternative is also investigated to develop a low-power one-stage LNA as a reference device.

3.3.1 Gain-boosting technique for millimeter-wave cascode amplifiers

Cascode amplifier stages are preferred for millimeter-wave applications [21]-[22], [30], because cascode stages have higher gain than single-transistor common-source/common-emitter (CS/CE) or common-gate/common-base (CG/CB) amplifiers. In addition, cascode amplifiers have decent noise performance. The transistor size and bias point can be optimized to bring noise and power matching conditions closer to each other [22]. However, the small-signal gain of the cascode core is much less (maximum available gain, i.e., $\text{MAG} < 10 \text{ dB}$) for lower-end IC processes (0.18 μm SiGe BiCMOS

or 0.13 μm CMOS). The transmission-line-based matching networks introduce significant additional loss (1.5-2.5 dB), and reduce the power gain of single-stage cascode amplifiers. This reduced power gain requires the application of gain-enhancement techniques to amplifier stages.

Gain boosting of a CG LNA has been reported at much lower RF frequency [41]. However, this technique requires a number of additional circuit components, and even then, it is not suitable for the cascode structure. There is also a report of cascode-gain boosting at lower RF frequencies [42], where a negative resistance generating circuit (MOS with gate inductance) is connected to the drain of the common-source (CS) MOS. However, this technique requires a separate transistor with additional biasing, and the bandwidth is narrow due to the tuned nature of the negative resistance generating circuit. In addition, this gain-boosting technique has inherent instability and higher oscillation possibility due to the parasitic effects at 60 GHz. There are other references [43]-[44] dealing with the stability and interstage matching of cascode devices. In this sub-chapter, a novel gain-boosting technique is proposed and analyzed [30]. This gain-boosting technique requires just one additional inductive feedback element to facilitate the layout and design complexity issues. A 0.18 μm SiGe HBT cascode amplifier is considered with the equivalent circuit of the transistor as shown in Figure 3.7 [45]. Next, we consider a single CB stage with an inductance in the base of the HBT as shown in Figure 3.8.

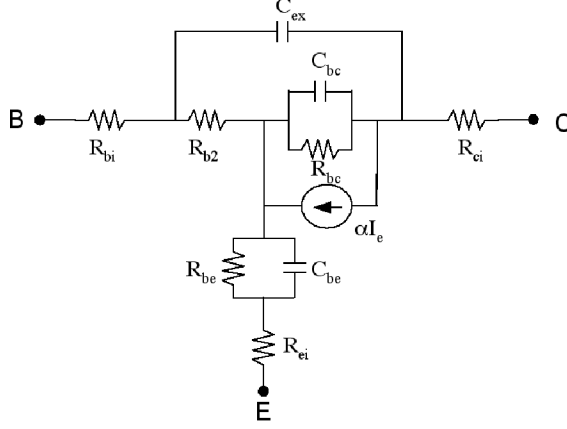


Figure 3.7. Gummel-poon based SiGe HBT small-signal model.

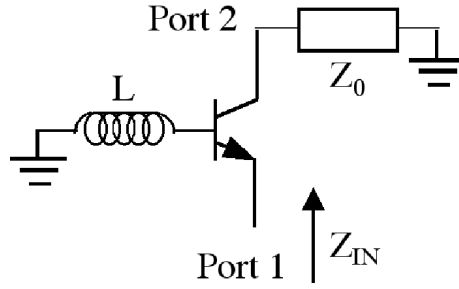


Figure 3.8. CB stage with base inductance.

The input impedance (Z_{IN}) can be determined in terms of two-port z -parameters and characteristic impedance (Z_0) as follows:

$$Z_{IN} = Z_{11} - \frac{Z_{12} \times Z_{21}}{Z_0 + Z_{22}} \quad (3.3)$$

The values of the z -parameters are

$$Z_{ij} = Z_{ij0} + j\omega L \quad \text{for } i = 1, 2; j = 1, 2; \quad (3.4)$$

Here, Z_{ij0} is the corresponding z -parameters in the absence of the inductance L , and ω is the frequency in radian.

Z_{IN} is determined as

$$Z_{IN} = Z_{IN0} + \Delta Z_{IN} \quad \text{where, } \Delta Z_{IN} = \frac{A \times j\omega L}{B^2 + B \times j\omega L} \quad (3.5)$$

Here,

$$A = \left[Z_0 + R_{ci} + \frac{1-\alpha}{j\omega \times (C_{ex} + C_{bc})} \right] \times \left[Z_0 + R_{ci} + \frac{1}{j\omega \times (C_{ex} + C_{bc})} - \frac{C_{bc} \times R_{b2}}{C_{ex} + C_{bc}} \right] \quad (3.6)$$

$$B = \left[Z_0 + R_{ci} + R_{bi} + \frac{1}{j\omega \times (C_{ex} + C_{bc})} \right] \quad (3.7)$$

The model parameters are extracted from the device (emitter length=6 μm) simulations [45], and the corresponding real and imaginary parts of Z_{IN} are plotted for different values of the base inductance (L). The evaluation of expressions based on this extraction is referred as model in the next few plots. Design kit simulations are referred as simulation. Figures 3.9(a) and 3.9(b) show the variation of Z_{IN} with the change in base inductance L .

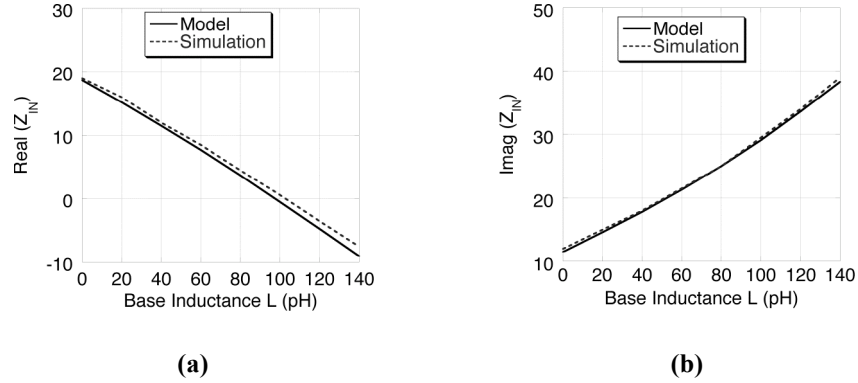


Figure 3.9. (a) Variation of real part of Z_{IN} with base inductance L in the CB stage; (b) Variation of imaginary part of Z_{IN} with base inductance L in the CB stage.

As shown in Figure 3.9, the real part of the input impedance of CB stage decreases, and the imaginary part of the input impedance of the CB stage increases with increasing base inductance (L) in an approximately linear fashion. This impedance acts as the load for the CE transistor in a cascode stage. To evaluate the effect of the base inductance on the CE stage, the voltage gain of the CE transistor with the varying load impedance is analyzed next.

The voltage gain of a CE stage can be defined in terms of its z -parameters and the load impedance (Z_L) as follows:

$$A_V = \frac{Z_{21} \times Z_L}{\Delta Z + Z_{11} \times Z_L} \quad (3.8)$$

Here, $\Delta Z = Z_{11} \times Z_{22} - Z_{12} \times Z_{21}$ (3.9)

The input impedance of the CB stage acts as the load impedance of the CE stage. Figure 3.10(a) plots the voltage gain of the CE stage for different real and imaginary values of Z_L over the entire range of input impedance of the CB stage ($V_{CE}=1.8$ V, $I_C=4.2$ mA). Figure 3.10(b) shows the voltage gain at specific impedances corresponding to different base-inductance values of the CB stage. The simulated voltage gain is also plotted to compare with the theoretical numbers, and they match reasonably well.

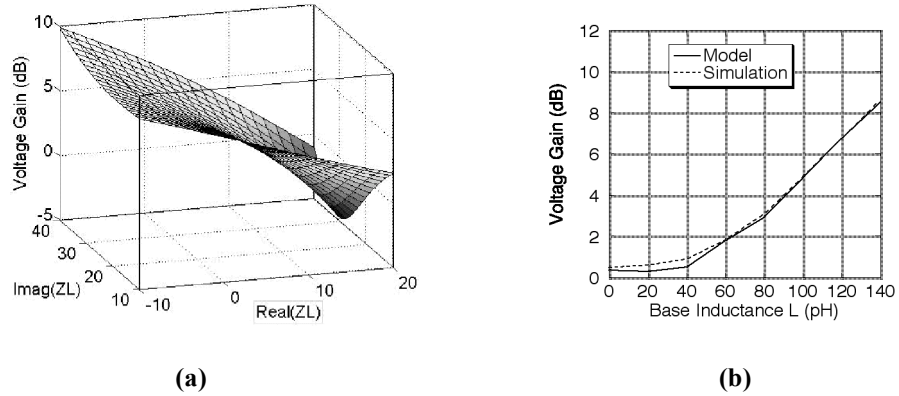


Figure 3.10. (a) Voltage gain of the given CE stage for different load impedances; (b) Voltage gain of the given CE stage with different base inductance (L) in CB stage.

Figures 3.10(a) and 3.10(b) imply that the voltage gain of the CE stage increases rapidly with the decrease in the real part of the load impedance and the increase in the imaginary part of the load impedance. This nature of the load impedance is caused by the base inductance in the CB stage. The power gain of the cascode stage increases due to this increase in the voltage gain of the CE stage. However, the voltage gain of the CB stage reduces (by a smaller extent), and limits the gain-enhancement using this technique

as shown later in Figure 3.11(b). Due to the complexity of the theoretical formulation of the power gain of the cascode as a function of CB stage base inductance (L), simulation results are considered as simulation trends match well with theoretical trends.

Figure 3.11(a) shows the schematic of the cascode core with the base inductance in CB stage. The emitter length is $6\text{ }\mu\text{m}$, and the DC conditions (derived from conditions of higher gain and lower DC power consumption) are mentioned. The variation of the corresponding MAG at 60 GHz with cascode base inductance is shown in Figure 3.11(b). Simulated s-parameters of the cascode core at 60 GHz are plotted with the variation of the base inductance in Figure 3.12.

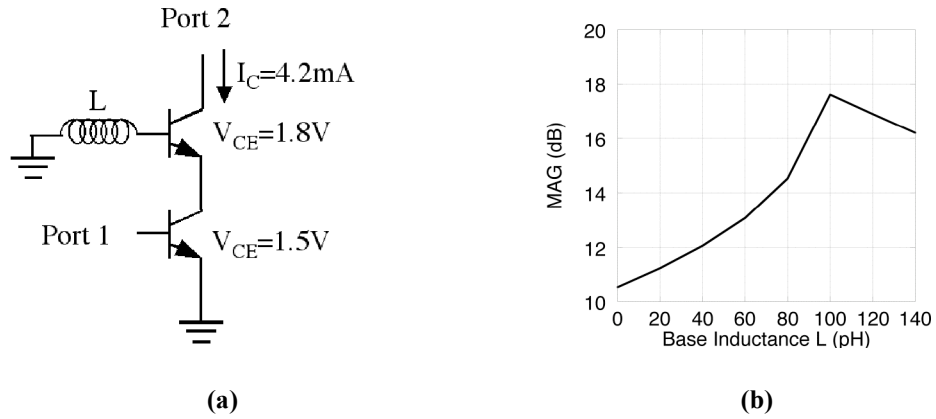


Figure 3.11. (a) Schematic of the cascode core; (b) Variation of MAG of the cascode core with base inductance (L).

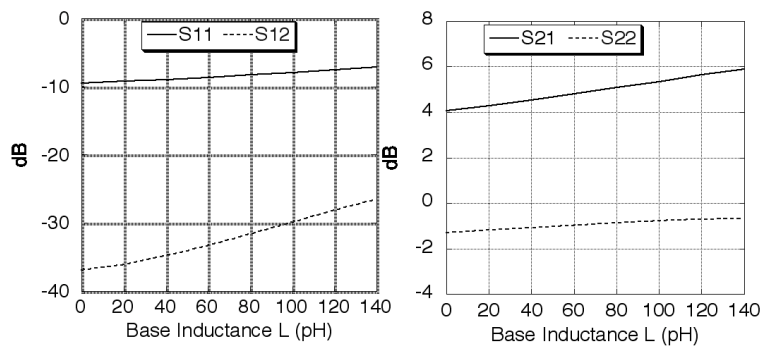


Figure 3.12. Simulated s-parameters of the cascode core at 60 GHz with different base inductance.

Figure 3.11 shows a significant improvement of MAG of the cascode core with the increasing inductance at the base of the CB transistor. This is due to the increase in voltage gain of the CE transistor. However, at higher values of L , MAG decreases by a small amount due to the reduction in gain of the CB stage. Hence, 90 pH has been chosen as the optimum base feedback inductance to enhance the gain of this particular cascode core. This enhances the simulated MAG by approximately 5 dB for the same power consumption.

Figure 3.12 shows an increasing trend in all the s-parameters with increasing L . This signifies a reduction in the overall stability factor (K) of the cascode stage, resulting in higher instability. The current consumption of the gain-enhanced cascode stage is reduced to increase the inherent stability factor. However, there is minimal shift in input matching (S_{11}), and hence, the noise matching condition and noise figure does not change significantly. Figure 3.13 shows the simulated frequency response of s-parameters of the cascode core with the selected base inductance. The nature of S_{22} (output matching) presents a stability concern at lower frequencies (approximately 40 GHz), but the bandpass nature of output-matching circuit prevents any instability in the amplifier stage.

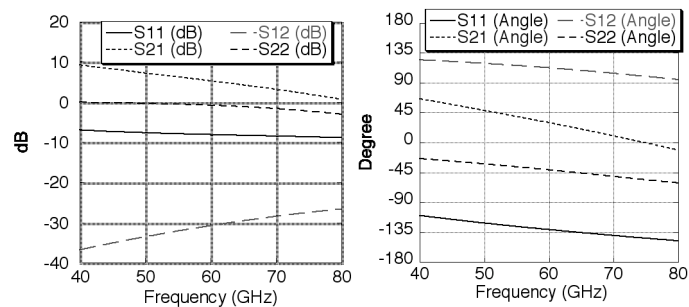


Figure 3.13. Frequency response of simulated s-parameters of the cascode core with 90 pH base inductance.

3.3.2 Gain-boosting implementation using 0.18 μm SiGe BiCMOS

The gain boosting technique is applied on a cascode LNA [30]. A microstrip transmission line is used to realize the feedback inductance at the base of the CB transistor in the cascode configuration. Figure 3.14(a) shows the schematic of the basic single-stage LNA, and Figure 3.14(b) shows the schematic of the gain-enhanced single-stage LNA. Both input-matching and output-matching networks use short-stub matching. Shorted stubs are also used to provide the base bias and supply voltage bias. The device size (6 μm) is selected to minimize the noise figure for power match and to minimize the DC power dissipation for a given gain.

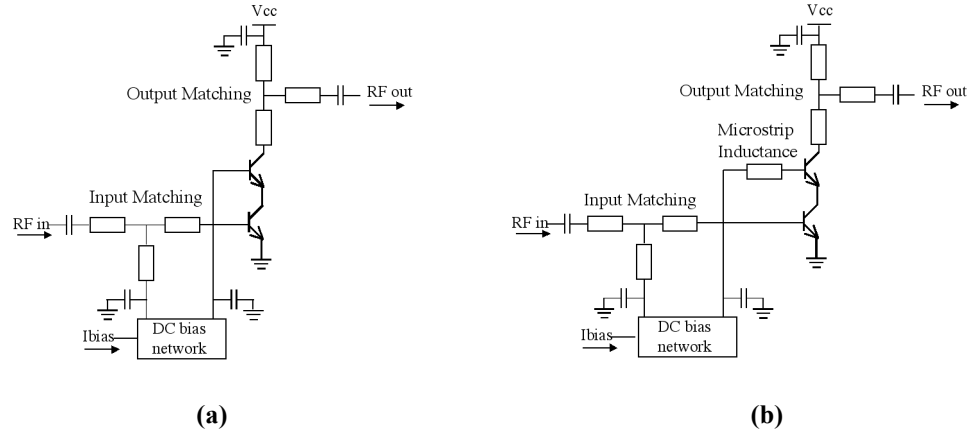


Figure 3.14. (a) Schematic of the conventional cascode LNA stage; (b) Schematic of the gain-enhanced cascode LNA stage.

The single-stage cascode LNA occupies an area of 0.86 mm \times 0.83 mm, and the gain-enhanced LNA occupies 1.05 mm \times 0.71 mm. The die photos of LNAs, fabricated in 0.18 μm SiGe BiCMOS process, are shown in Figure 3.15(a) and Figure 3.15(b).

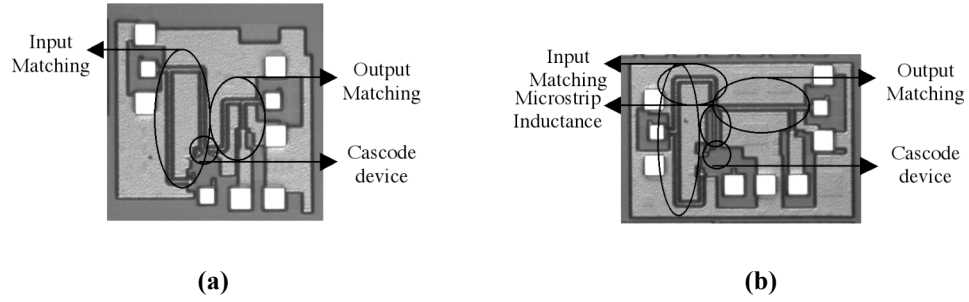
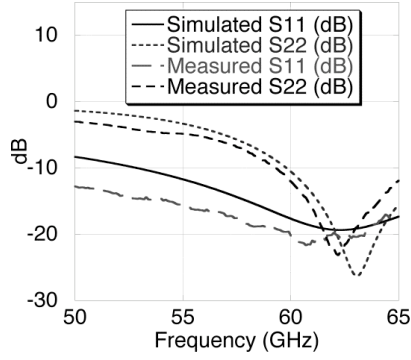
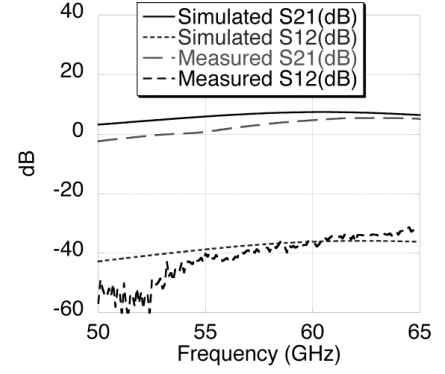


Figure 3.15. (a) Die photograph of the conventional cascode LNA stage; (b) Die photograph of the gain-enhanced cascode LNA stage.

The cascode stage without gain boosting is measured to have a higher than 5 dB gain at 60 GHz band with a 1-dB bandwidth above 7 GHz as shown in Figure 3.16. The DC power consumption is 16.5 mW (5 mA from 3.3 V supply). Resistive losses of transmission lines are not taken into account in the simulation, and they account for the approximately 2 dB difference between the measured gain and the simulated gain. The gain-enhanced cascode LNA is measured to have a higher than 9 dB stable gain (K factor >1.4 over the frequency range) with a 1-dB bandwidth greater than 6 GHz as shown in Figure 3.17. The DC power consumption is 13 mW (3.5 mA from 3.7 V supply). Hence, the gain-enhancement technique results in a higher than 4 dB gain improvement at 60 GHz for similar area and DC power consumption. The shift in the output matching is primarily caused by the parasitic inductance ($\sim 25\text{-}30$ pH) in the feedback path and higher than predicted inductive effects. The measured output P1dB is approximately -3.5 dBm for both cases. Figure 3.18(a) shows the measured and simulated linearity of the gain-enhanced cascode stage at 60 GHz. They correspond well with each other. The simulated noise figure of the gain-enhanced cascode stage is slightly higher (~ 0.5 dB) than that of the basic cascode stage. Figure 3.18(b) compares simulated noise figures of two different configurations.

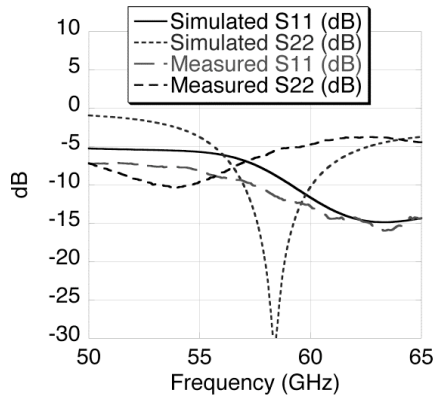


(a)

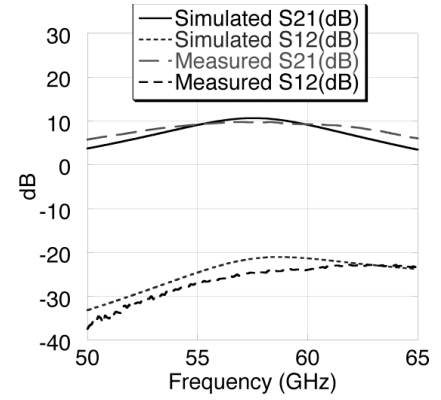


(b)

Figure 3.16. (a) Measured and simulated S_{11} and S_{22} of the conventional cascode LNA; (b) Measured and simulated S_{21} and S_{12} of the conventional cascode LNA.

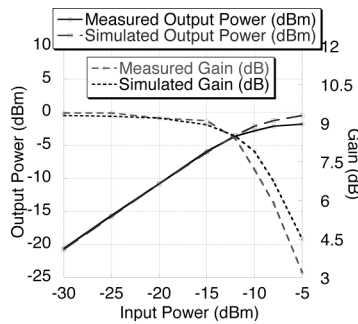


(a)

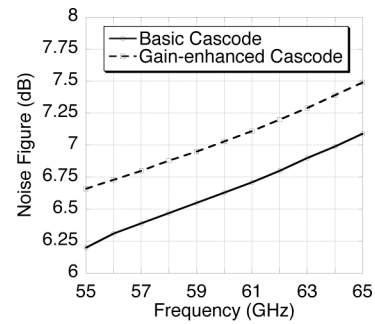


(b)

Figure 3.17. (a) Measured and simulated S_{11} and S_{22} of the gain-boosted cascode LNA; (b) Measured and simulated S_{21} and S_{12} of the gain-boosted cascode LNA.



(a)



(b)

Figure 3.18. (a) Measured and simulated linearity of the gain-enhanced cascode LNA; (b) Simulated noise figure of two different cascode stages.

3.3.3 Low-power front-end LNA design using 0.18 μm SiGe BiCMOS

One basic cascode stage and two gain-enhanced cascode stages are cascaded to implement a three-stage LNA that can be used in the low-power front-end [30]. The gain-boosting technique is not applied to the first stage in order to minimize the noise figure of the integrated LNA. Fig. 3.19 shows the schematic of the 3-stage LNA. The die photograph of the fabricated LNA is shown in Fig. 3.20. It occupies an area of $2.05\text{ mm} \times 0.71\text{ mm}$.

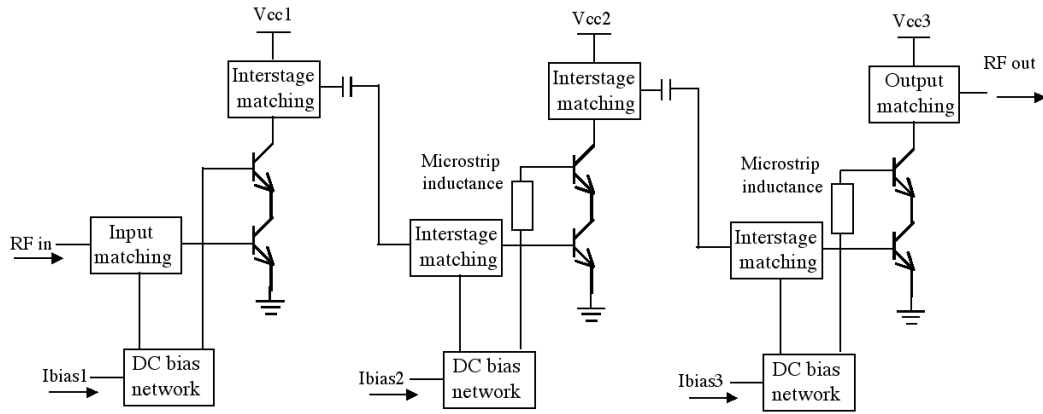


Figure 3.19. Schematic of the three-stage LNA.

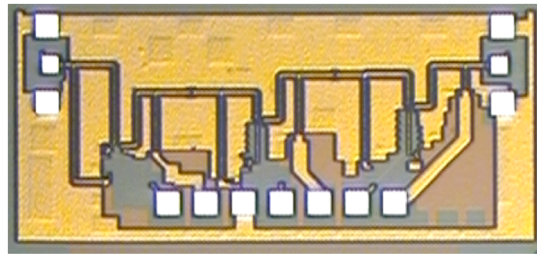


Figure 3.20. Die photograph of the gain-boosted three-stage LNA in 0.18 μm SiGe.

Measurement results show a higher than 24 dB stable gain (K factor > 4 at the measured frequency range) at 60 GHz with a 3.1 GHz 3-dB bandwidth for a DC power consumption of 25 mW. The measured noise figure is 7.9 dB at 60 GHz, and is shown in

Figure 3.21. The output P1dB is a little lower than the gain-boosted stage because of the reduction of the DC bias current in the last stage, and is approximately -5 dBm at 60 GHz. The measured and the simulated s-parameters are shown in Figure 3.22. Table 3.1 compares the performance this LNA with other recently reported silicon-based 60GHz LNAs. The LNA reported in this work shows the highest gain at a very low DC power consumption. Also, this is the only reported LNA in a $0.18\text{ }\mu\text{m}$ silicon-based process.

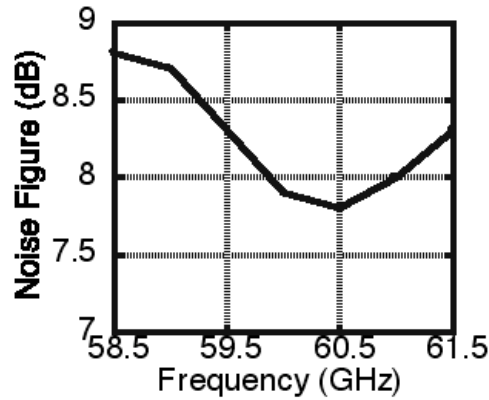


Figure 3.21. Measured noise figure of the three-stage LNA.

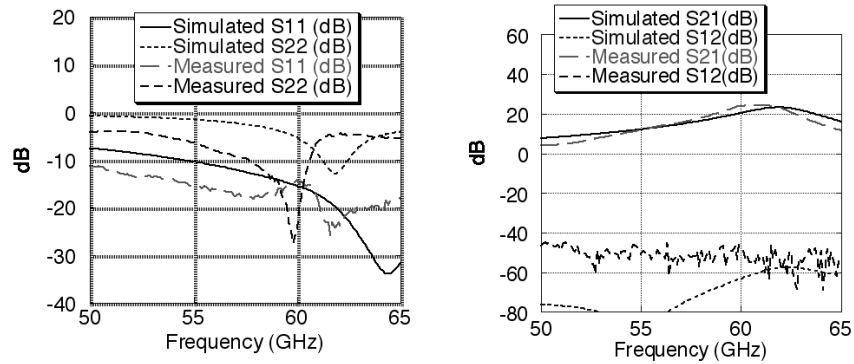


Figure 3.22. Measured and simulated s-parameters of the three-stage LNA.

Table 3.1. Comparison of silicon-based 60 GHz LNAs.

Process [Ref]	Topology	Frequency (GHz)	Gain (dB)	Noise Figure (dB)	DC Power (mW)	Output P1dB (dBm)
0.12 μ m SiGe HBT[20]	1-stage CG + caocode	56-64	15	4.5	11	-5@ 61GHz
0.13 μ m CMOS [21]	3-stage cascode	51-57	>20	~8	72	1.8@ 56GHz
0.13 μ m CMOS [10]	3-stage cascode	51-65	12	8.8	54	2@ 60GHz
90nm CMOS [22]	2-stage cascode	55-60	14.6	5.5	24	-0.5@ 58GHz
90nm CMOS [23]	2-stage CS	NA	12	6	12	4 @60 GHz
0.18 μ m SiGe [This work] [30]	3-stage cascode [modified]	58-63	24	7.9 @60 GHz	25	-5@ 60GHz

3.3.4 Low-power front-end LNA design using 0.12 μ m SiGe BiCMOS

The development of low power LNA with standard cascode topology is investigated in 0.12 μ m SiGe process. A cascode LNA with transmission line-based input-matching and output-matching structures has been implemented. The matching networks are similar in nature as the matching networks implemented in the previous sub-chapters. An inductive degeneration has been used with a small transmission line, and the current consumption is minimized to realize a low-power design. The DC bias has been provided through the short stubs in the matching network in order to minimize the layout area. The stubs are shorted using the decoupling capacitors on chip. The emitter lengths of transistors are 7 μ m. Figure 3.23(a) shows the schematic of the LNA, and Figure 3.23(b) shows the die photograph of the LNA. The LNA occupies 1.12 mm \times 0.65 mm. The measurement results show a gain of 7 dB at 60 GHz for a DC power consumption of 5 mW only (2.5 mA from 2 V power supply). The measured s-parameters are shown in

Figure 3.24. The simulated noise figure is around 5 dB at 60 GHz. The measured output P1 dB is around -3 dBm.

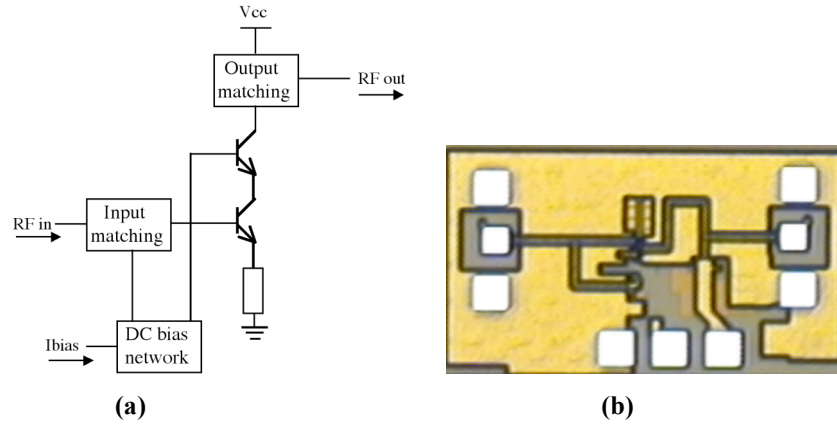


Figure 3.23. (a) Schematic of the one-stage LNA; (b) Die photograph of the one-stage LNA.

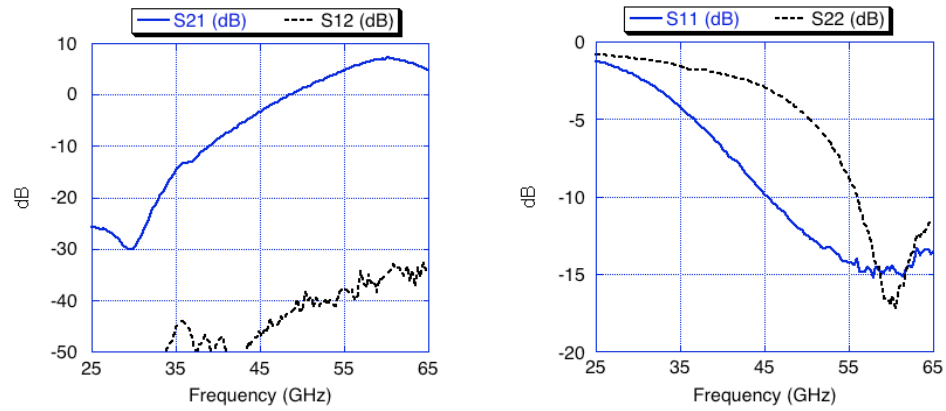


Figure 3.24. Measured s-parameters of the one-stage LNA.

3.4 Low-power non-coherent amplitude-detection scheme

Amplitude detection is the simplest demodulation scheme. The non-coherent amplitude-modulation scheme does not require any external LO or synchronization. However, amplitude-detection has a worse SNR compared to coherent schemes as shown in chapter 2. Still amplitude detection is suitable for moderate data rate, small distance, and low-cost links [17].

A reverse-biased diode is suitable for square-law detection. A DC bias current shifts the DC quotient of the diode to reduce the conversion loss. The choice of device size and bias current depends on the trade-off of following specifications:

- i. Minimum conversion loss
- ii. Maximum bandwidth
- iii. Highest sensitivity
- iv. Minimum second harmonic distortion

The amplitude-modulated signal may be represented as $A(1+m(t))\cos(\omega_c t)$, where the carrier signal is $A\cos(\omega_c t)$, and the modulating signal is $m(t)$. For a sinusoidal modulating signal $B\sin(\omega_m t)$, the modulated signal becomes

$A\cos(\omega_c t) + \frac{AB}{2}(\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t)$. Figure 3.25 shows the basic schematic of the detector core with baseband buffer stages [30]. The input matching of the detector diode and the bandwidth of the baseband buffer determines the overall data bandwidth for this detection scheme.

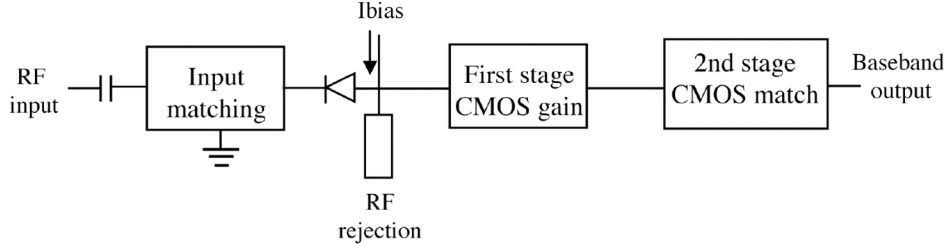


Figure 3.25. Schematic of the diode-based amplitude detector.

The operating point of the diode in the absence of the input RF signal is set by the bias voltage (V_b), and the bias current is

$$I_b = I_0(e^{V_b/\eta V_T} - 1) \quad (3.10)$$

Here, I_0 is the reverse saturation current. When the amplitude-modulated signal (V_i) is present, the instantaneous total current flow through the diode is

$$I = I_0(e^{(V_b - V_i)/\eta V_T} - 1) \quad (3.11)$$

The negative sign indicates the reverse bias nature of the diode. If the load of the detector is R_L (considering the series resistance of the bias path and neglecting the loading effect of buffer stages), the following relation can be established;

$$\frac{V_i}{\eta V_T} = \ln(i + 1) + P i \quad (3.12)$$

Here, $P = R_L / R_d$ (R_d being the dynamic resistance of the diode $= dI/dV$), and i is normalized incremental current ($i = (I - I_b) / (I_b + I_0)$).

Thus, the incremental instantaneous current (i) can be represented as a Taylor series expansion of $(V_i/\eta V_T)$, i.e., a linear function of the input RF voltage. The contribution of coefficients decreases with the increasing order of the series. The second-order term contributes to the reconstruction of the original modulating signal. The baseband buffer also acts as a low pass filter that eliminates the linear term, i.e., frequency components

around carrier frequency (60 GHz). The bias current and dynamic resistance determines the strength of the higher-order terms, and with the increasing bias current, their strength and resultant non-linearity increases. The reverse-biased configuration is preferred for the two following reasons:

- i. The input matching of the detector is easier;
- ii. If the input signal power is increased (e.g. bringing transmitter and receiver too close to each other), the output voltage of the diode reduces and hence prevents any kind of breakdown of the baseband buffer stage (there is no capacitive coupling between the diode and CMOS buffer stage).

In addition, a CMOS baseband buffer is used because the baseband chain is DC coupled. In case of HBT stages, a small DC shift would change operating conditions to a large extent. A large off-chip series capacitor can be used to decouple the output from the subsequent baseband-processing stages.

The implementation of the amplitude detector is targeted in the low-cost 0.18 μm SiGe BiCMOS process. Base-collector shorted n-p-n SiGe HBTs are used as diodes [29]. The cut-off frequency of the diode is simulated to be higher than 250 GHz. A very small device length (1 μm) with the minimum width (0.18 μm) is selected to minimize the device capacitance, and hence, to enhance the baseband bandwidth. The second stage of the buffer has a 50 Ω load impedance so that the output impedance becomes 50 Ω . Figure 3.26 shows the simulated conversion characteristics of the input-matched detector (excluding the buffer) at different bias currents. The input is considered to be a perfectly modulated (modulation index=1) 60 GHz carrier. The output is the diode-forward-biased node voltage considering the loading effect of the buffer.

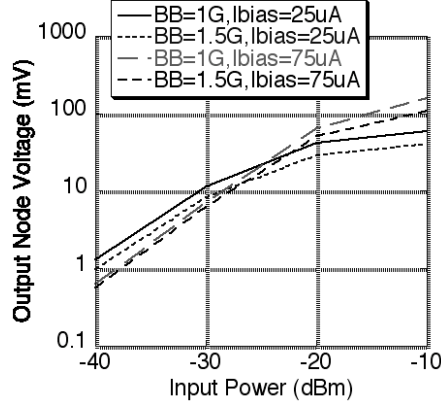


Figure 3.26. Simulated conversion characteristics of the amplitude detector (60 GHz carrier).

From the conversion characteristics, it can be seen that the conversion gain and bandwidth depends on the bias current. The nominal bias current is chosen to be 50 μA . Figure 3.27(a) shows the die photograph of the amplitude detector test structure. Figure 3.27(b) shows the measured input matching of the detector at different bias points. The measurements for conversion characteristics have been performed in the integrated receiver front-end, and measurements have been summarized in sub-chapter 3.7.

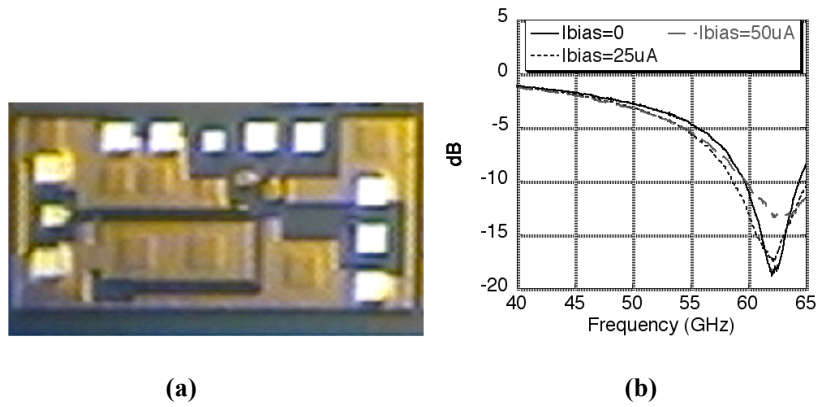


Figure 3.27. (a) Die photograph of the amplitude detector in 0.18 μm SiGe; (b) Measured input matching of the amplitude detector.

3.5 Passive subharmonic mixing scheme

The subharmonic mixing scheme requires a lower frequency oscillator, and is also broadband in nature [29]. The passive subharmonic mixing scheme is also suitable for a low-power front-end, because the mixer does not draw any DC current. However, the passive subharmonic mixers have its drawbacks in terms of the conversion loss and higher LO power requirement, but at a lower LO frequency. The high-gain front-end amplifiers, as discussed in the previous section, can compensate the conversion loss of the mixer.

The mixer implementation primarily targets 0.12 μm SiGe BiCMOS process because of the expected performance of diodes compared to 0.18 μm SiGe BiCMOS. At first, a proof-of-concept subharmonic mixer is implemented in 0.12 μm SiGe. Subsequently, the same design is translated into 0.18 μm SiGe with an on-chip oscillator for the LO signal generation. The primary reasons for the selection of the 2X mixer over the 4X mixer in silicon are as follows:

- i. Additional requirements of the rejection network for the 4X mixer (suppression of 2X-mixing components) increase the area of the mixer. Silicon-die area should be kept minimum for the low-cost integration.
- ii. Conversion loss of 2X mixer is approximately 6 dB less than 4X mixer if properly designed.
- iii. Diodes available in a silicon process (created by shorting base and collector terminal of a SiGe HBT) generate less non-linearity compared to GaAs diodes. This effect might reduce the strength of the 4X-mixing term.

- iv. There have been several reports of a reliable 30 GHz (and higher frequency)-signal generation [46]-[47] on silicon, and hence 2X mixing is sufficient to obtain advantages of the passive subharmonic mixing.

Figure 3.28(a) shows the schematic of the 2X subharmonic mixer developed using 0.12 μm SiGe BiCMOS process. Figure 3.28(b) shows the photo of the fabricated mixer. This mixer has been optimized for direct-conversion architecture.

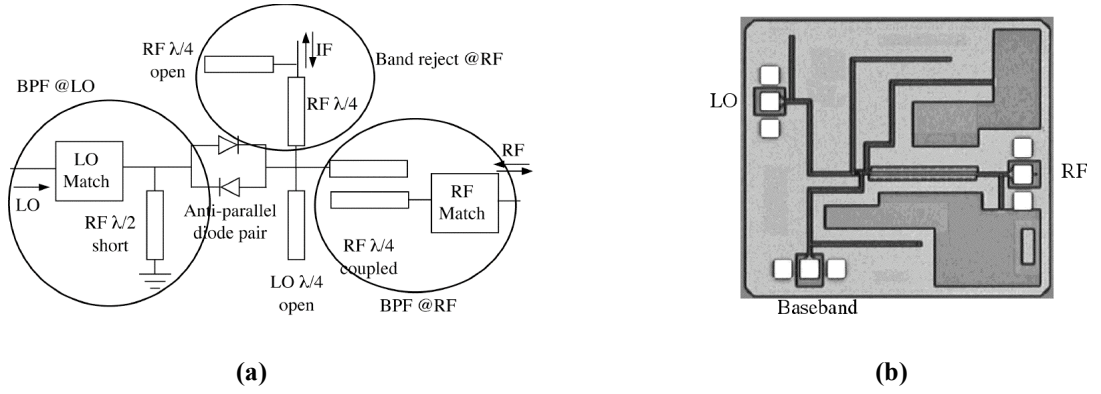


Figure 3.28. (a) Schematic of 2X mixer in 0.12 μm SiGe; (b) Photo of the fabricated mixer.

All the transmission lines are realized in CB-CPW mode to minimize the radiation loss as compared to the microstrip implementation. Only the RF $\tilde{\lambda}/4$ -coupled section is microstrip to avoid the possibility of mixed propagation modes. In Figure 3.28(a), the encircled portion in the left is essentially a bandpass filter at LO frequency (30 GHz). The RF (60 GHz) $\lambda/2$ -shorted stub acts as a short circuit for both RF and baseband frequencies, but presents an open circuit for the LO frequency. Hence, RF and baseband signals cannot leak to the LO source. Similarly, the $\tilde{\lambda}/4$ -open stub at LO frequency in the other side of the APDP acts as a short for LO and open for RF and baseband. Hence, the entire LO signal is available across the diode pair. An additional LO-matching network

has been implemented to minimize the return loss from the LO source. As a result, LO-power requirements are minimized. In Figure 3.28(a), the encircled portion in the right is essentially a bandpass filter at RF frequency (57-64 GHz). The bandpass filter contains one $\tilde{\lambda}/4$ -coupled-microstrip section at RF and additional matching network to minimize the return loss from the RF port. The coupled section prevents baseband signal leaking to the RF port. In Figure 3.28(a), the encircled portion in the top is a RF band-reject filter constituting a RF $\tilde{\lambda}/4$ -transmission line followed by a RF $\tilde{\lambda}/4$ -open stub. The band-reject filter shows an open circuit to RF signals, and prevents RF signal leaking to baseband port. The mixer takes an area of $1.4\text{mm} \times 1.5\text{mm}$.

Base and collector terminals in an n-p-n HBT are shorted in order to transform it into a p-n diode. Another option to realize a diode is shorting base and emitter terminals. However, the first configuration has substantially higher non-linearity at a lower input voltage, and also a much less series resistance compared to the second option as determined by simulations. The series resistance and the junction capacitance of the diode under zero-bias condition are critical to determine the emitter length of transistors in the diode configuration. There is a direct trade-off as the series resistance decreases, and the junction capacitance increases with the increase in the transistor size. Figure 3.29(a) shows the zero-bias series resistance and junction capacitance with increasing emitter length. An emitter length of $3\text{ }\mu\text{m}$ is selected for implementation. Figure 3.29(b) shows the measured and simulated APDP s-parameters with the selected diode.

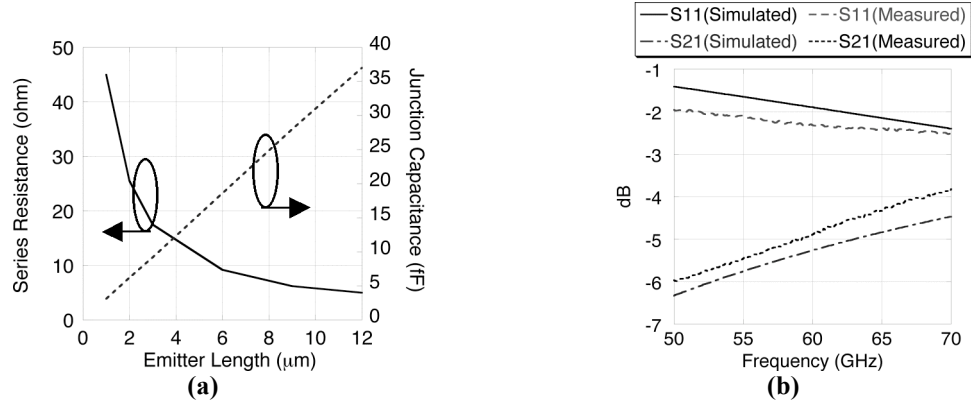


Figure 3.29. (a) Diode characteristics with different emitter lengths; (b) Measured and simulated s-parameters of the APDP.

The mixer has been measured in a down-conversion setup. The mixer has a minimum conversion loss of 8.3 dB with a greater than 9GHz of 3-dB double-sided (DSB) baseband bandwidth with a 5.5 dBm 30.5 GHz LO signal [29]. The conversion loss includes about 2 dB loss in the coupled section. This is an excellent conversion loss performance in consideration of the theoretical limits of 2X APDP-based mixing [33]. Figure 3.30 shows the comparison of the simulated and the measured conversion loss with the variation of (a) RF frequency (at -26 dBm RF power level) and (b) RF power (at 62 GHz RF frequency) with the same LO signal. The input 1dB-compression point has been measured as -7 dBm. Figure 3.31(a) shows the measured and simulated conversion loss with the variation of LO frequency (power level of 5.5 dBm) for a fixed baseband frequency (1 GHz). The mixer shows less than 10 dB measured conversion loss for a LO frequency range of 28-32 GHz. Figure 3.31(b) describes the variation of the conversion loss with LO power and the corresponding LO leakage in the baseband output. Typically, this mixer provides 35 dB isolation between the LO and baseband ports. The simulated estimate of the noise figure (NF) of the subharmonic mixer is approximately 12 dB. The measured return loss of the RF port corresponds well to the simulation as shown in

Figure 3.32. The measurement in the upconversion setup of the mixer exhibits a similar conversion-loss performance of the 2X mixer.

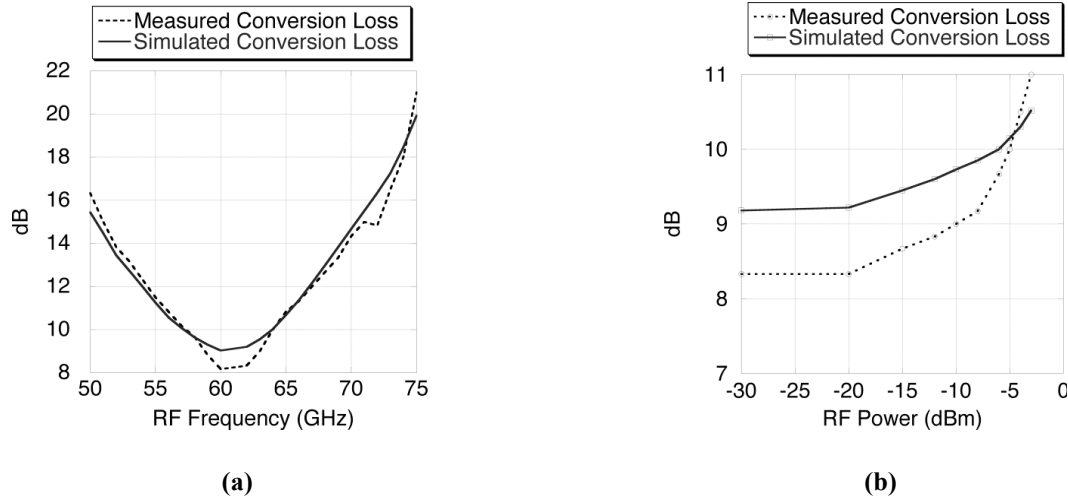


Figure 3.30. (a) Conversion loss of the mixer with RF frequency; (b) Conversion loss of the mixer with RF power.

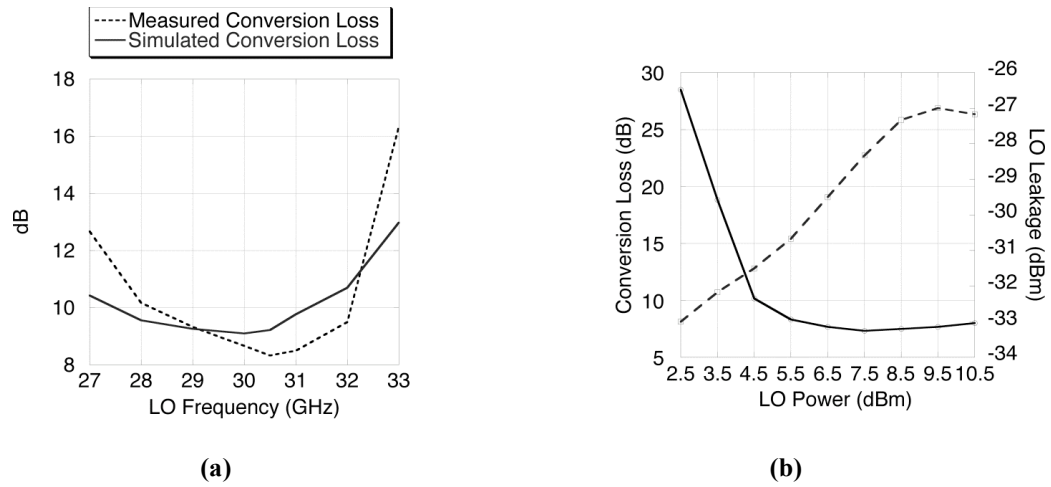


Figure 3.31. (a) Conversion loss of the mixer with LO frequency; (b) Conversion loss of the mixer with LO power.

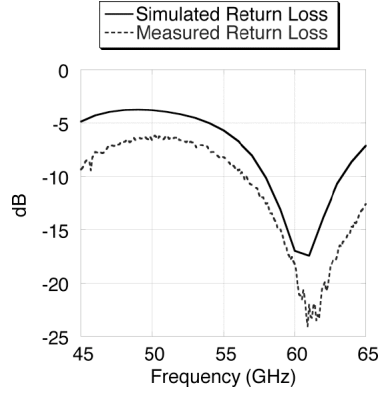


Figure 3.32. Measured and simulated RF-port matching of the subharmonic mixer.

Table 3.2 compares the implemented subharmonic mixer with recently reported silicon-based millimeter-wave mixers, as well as a few of other integrated 40/60 GHz subharmonic mixers. The 2X mixer shows an excellent conversion loss and bandwidth performance. The implemented mixer has the highest DSB bandwidth among the reported 60 GHz mixers (required for broadband systems), and the lowest conversion loss among the reported millimeter-wave subharmonic mixers.

Table 3.2. Comparison of millimeter-wave mixers.					
Process [ref. no.] and topology	Conversion gain/loss (dB)	3-dB Bandwidth (GHz)	LO power (dBm)	DC power (mW)	Input P _{1dB} (dBm)
SiGe [48] Gilbert cell	11	7.5-11 SSB IF	-4@RF diff.	19.2	-7
CMOS [26] single gate	-2	6GHz DSB	0@ RF	2.4	-3.5
SiGe [49] (77GHz) 2X balanced	3	0.1-1 SSB IF	10 @RF/2	62	-8
GaAs [35] 4X APDP	-13	1.5-2.5 SSB IF	7 @RF/4	0	-
Duroid + GaAs diode [50] (40GHz) 2X APDP	-14	0.5GHz DSB	12 @RF/2	0	-
InP [51] 2X APDP	-12	4-12 SSB IF	13 @RF/2	0	-
LCP + GaAs diode 4X APDP [27]	-17	2.5GHz DSB	8.5 @RF/4	0	-2
<i>SiGe 2X APDP [29]</i>	-8.3	9GHz DSB	5.5@RF/2	0	-7

The subharmonic mixer design is translated into 0.18 μm SiGe BiCMOS process with the RF coupled line replaced by a MIM capacitor to reduce the die area. In addition, the matching networks are tuned to optimize the mixer for an IF of 1-6 GHz instead of direct-conversion. This subharmonic mixer demonstrates its potential in a compact and low-power heterodyne front-end. The LO port of the mixer is fed by an on-chip cross-coupled VCO followed by a cascode amplifier. The VCO is tuned at 29 GHz LO frequency that will generate an IF of 1-6 GHz for the 59-64 GHz frequency band. The emitter length of transistors in the diode pair is selected as 6 μm . Figure 3.33 shows the schematic of the subharmonic mixer. Figure 3.34 shows the die photograph of the integrated subharmonic mixer with the cross-coupled VCO and LO amplifier. The total die area is only 1.4 mm \times 1.2 mm. Figure 3.35 shows the die photograph of the VCO-mixer.

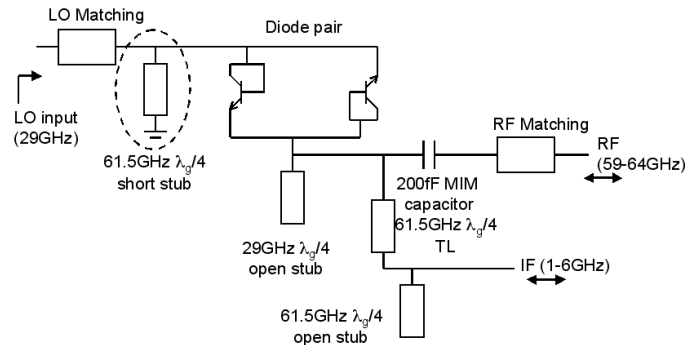


Figure 3.33. Schematic of the compact passive 2X subharmonic mixer.

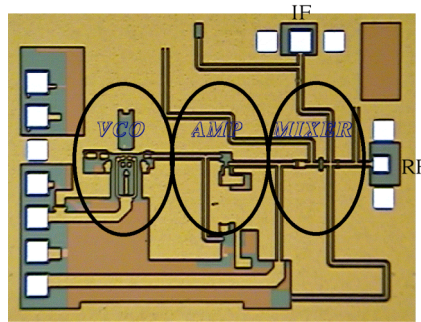


Figure 3.34. Die photograph of the integrated VCO-subharmonic mixer.

The VCO-Mixer has been measured in both up and downconversion scenario. The mixer is measured to have an 11.5 dB conversion loss for 1 GHz IF in downconversion. For upconversion, the corresponding conversion loss is 11 dB. The optimum LO frequency generated by the VCO is shifted to 30.5 GHz. The VCO with the amplifier consumes less than 40 mW DC power. The mixer achieves a double-sided bandwidth of 9 GHz. The single-sided bandwidth (SSB) is approximately 5.5 GHz in the lower band and 3.5 GHz in the higher band. The measured input P1-dB of the mixer is -2 dBm. The measured noise figure during downconversion is approximately 16 dB. Figure 3.35(a) shows the measured downconversion loss for a VCO-oscillation frequency of 30.5 GHz. Figure 3.35(b) shows the measured upconversion loss for a VCO-oscillation frequency of 30.5 GHz. The LO power generated by the VCO was less than the nominal value, and that causes a few dB higher conversion loss.

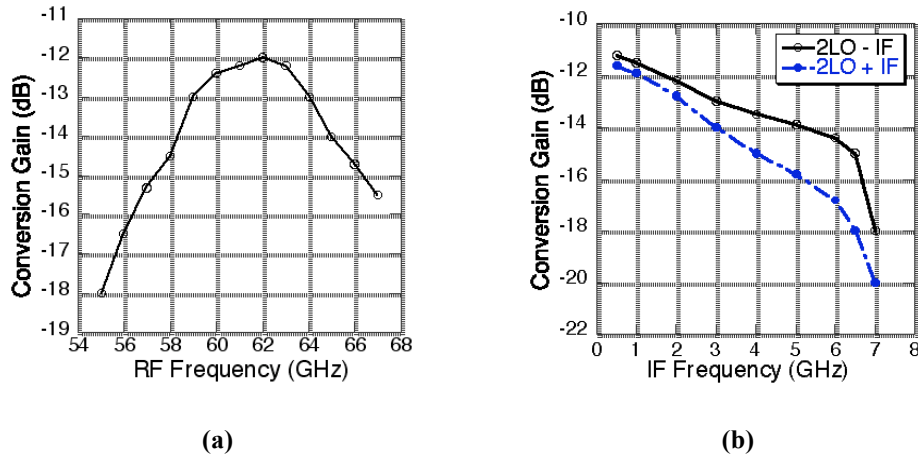


Figure 3.35. (a) Downconversion loss of the mixer with RF frequency; (b) Upconversion loss of the mixer with IF frequency.

The passive subharmonic mixing scheme is successfully implemented in both 0.18 μm and 0.12 μm SiGe BiCMOS processes. Also, this mixing scheme is realized for both downconversion and upconversion mixers. Although this mixing scheme is inherently

suitable for direct downconversion, a modified version for heterodyne architecture is also demonstrated. In addition, an integrated VCO-mixer is shown to demonstrate the potential of integrated 60 GHz front-ends.

3.6 60 GHz multi-gigabit receiver integration in 0.18 μm SiGe

Two different 60 GHz receiver integrations have been demonstrated in this sub-chapter. Both of them are suitable for low-power and low-cost integration. A 0.18 μm SiGe platform has been chosen to ensure lower cost. The first alternative targets non-coherent ASK demodulation, and the second alternative demonstrates a passive subharmonic heterodyne front-end (can also be used in a direct-conversion architecture). The gain-boosted front-end LNA, describes in Chapter 3.3, has been used to enhance the gain of the front-end amplifier and to compensate for the conversion-gain characteristics of the amplitude detector and the passive subharmonic mixer. The ASK multi-gigabit receiver front-end IC is integrated in an LCP-based organic package to develop a low-cost 60 GHz receiver module.

3.6.1 Integrated 60 GHz antenna-to-baseband multi-gigabit ASK receiver

The three-stage LNA (described in chapter 3.3) is integrated with the amplitude detector (described in chapter 3.4) to develop the direct-conversion non-coherent receiver [30]. This integration is the most low-power solution because the receiver does not require any voltage controlled oscillator or PLL blocks. The monolithic integration, i.e., the receiver IC, is also combined with the low-cost organic-based module integration to develop the complete antenna-to-baseband solution. The module fabrication follows standard PWB techniques suitable for high-volume, large-area integration. Figure 3.36 shows the block diagram of the 60 GHz receiver module. The die area of the integrated ASK receiver chip is only $3\text{mm} \times 1\text{mm}$. The effective area of the module is only $8\text{ mm} \times 18\text{ mm}$.

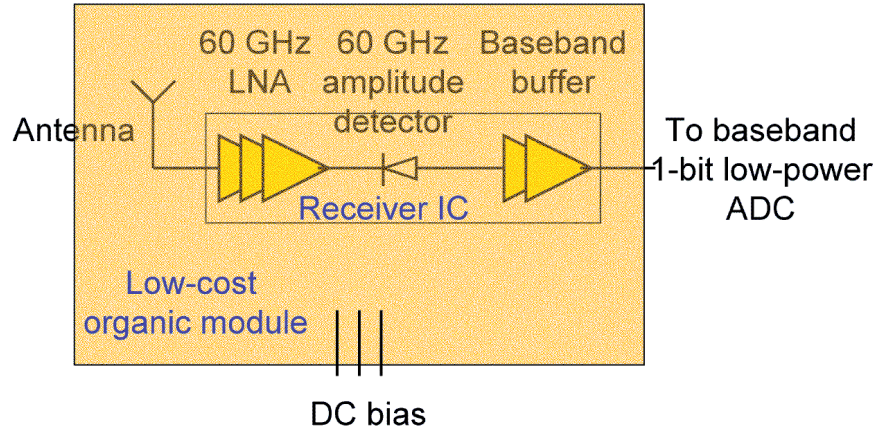


Fig. 3.36. Block diagram of the 60 GHz ASK receiver module.

The output matching of the three-stage LNA and the input matching of the amplitude detector are modified to design the interstage-matching network in between the LNA and the amplitude detector. The total power consumption of the integrated receiver IC is only 37 mW (25 mW for the LNA, negligible for the detector, and 12 mW for the baseband buffer). The die area of the integrated ASK receiver chip is only 3mm × 1mm. Figure 3.37 shows the die photo of the receiver chip. Figure 3.38 shows the photograph of the module. A FR4/LCP-based low cost substrate is used. The effective area of the module is 8mm × 18mm.

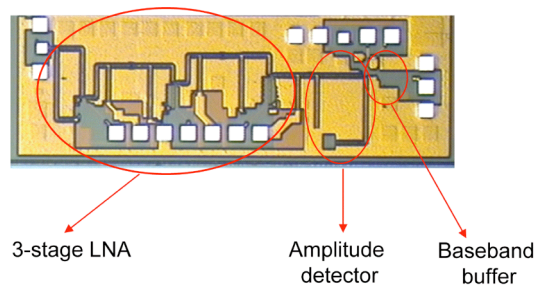


Figure 3.37. Die photograph of the integrated 60 GHz ASK receiver IC.

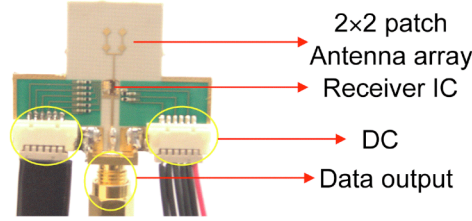


Figure 3.38. Photograph of the 60 GHz ASK-receiver module.

A two-by-two circularly polarized patch-antenna array is printed on the organic board. This circularly polarized antenna has a good multi-path resistance to reduce the interference from reflections. The 3-dB axial-ratio bandwidth of this antenna is more than 2 GHz. Figure 3.39(a) shows the simulated and measured s-parameter of this antenna. Figure 3.39(b) shows the measured relative gain with the angle (maximum gain is 10 dBi) and the simulated radiation pattern.

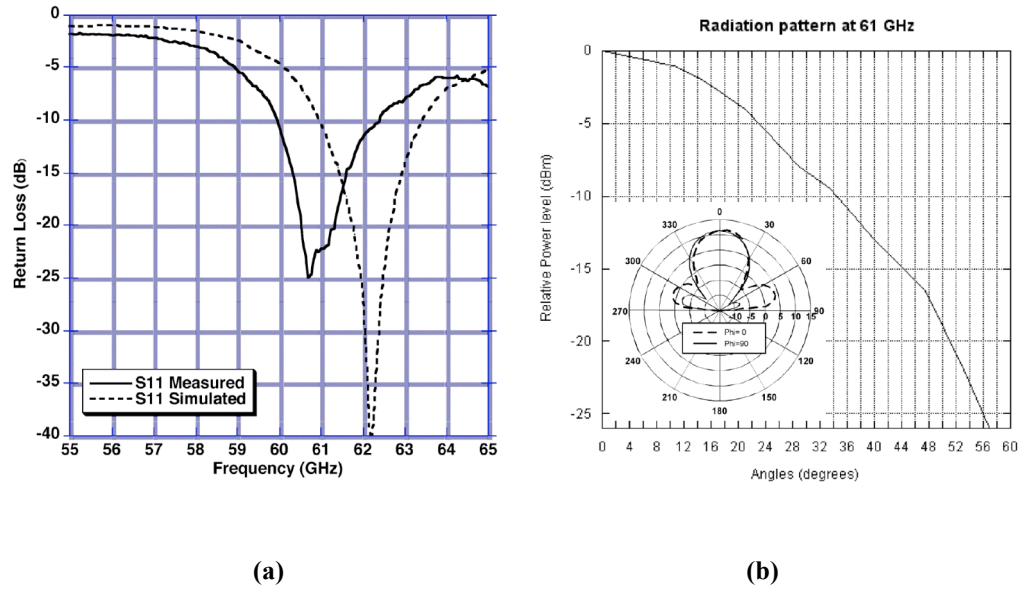


Figure 3.39. (a) Measured and simulated s-parameters of the antenna; (b) Measured relative gain of the antenna.

For test purposes, a transmitter module is implemented using commercial components with 10 dBm of output power and a similar two-by-two circularly polarized patch-

antenna array. The receiver successfully demodulates up to 1.5 Gbps pseudo-random-binary-sequence (PRBS) for a greater than 2 meters distance from the transmitter. The complete DC power consumption of the receiver is 37mW, i.e., 25pJ/bit only. The output of the module is direct analog data, and this output can directly be connected to a one-bit ADC (inverter or comparator) for digital data recovery. Figure 3.40 shows the eye-diagram of the received 1.5 Gbps data for a link distance of 1.5 meter between the transmitter and the receiver.

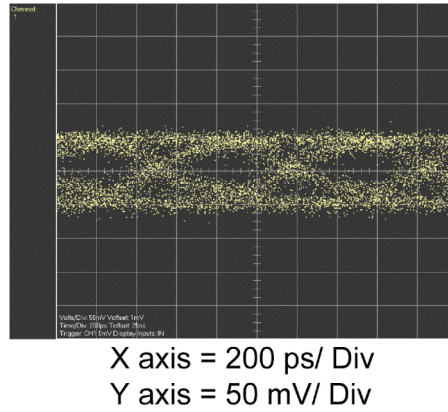


Figure 3.40. Received eye diagram for 1.5 Gbps PRBS at 1.5 m wireless link distance.

The received raw data corresponds to a BER of 10^{-5} , and this BER can be improved by error-correction schemes and equalization. However, the most critical achievement of this front-end is to develop an ultra low-power complete 60 GHz solution at a power budget that is at least one order of magnitude lower than other reported 60 GHz publications, and also lower than the communication data-rate vs power budget trend. Figure 3.41 shows the power budget of different wireless communication schemes along with the scheme reported in this work.

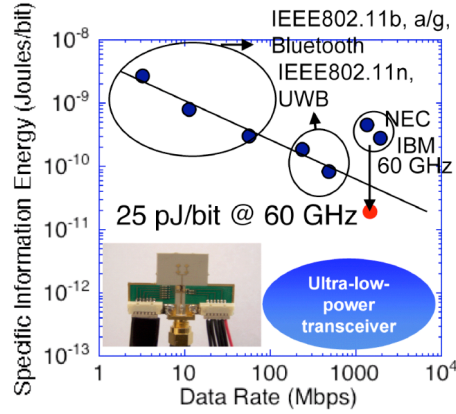


Figure 3.41. Power-budget vs. data-rate comparison of existing wireless standards and 60 GHz receivers with the reported 60 GHz receiver.

3.6.2 Integrated 60 GHz subharmonic receiver front-end in 0.18 μm SiGe

A subharmonic heterodyne receiver front-end is developed in 0.18 μm SiGe BiCMOS process. The gain-boosted three-stage LNA is integrated with the 2X passive subharmonic mixer for the heterodyne front-end. The front-end can also be fine tuned for a direct-downconversion architecture. The single-chip integration has been performed by modifying the output-matching network of the LNA and the RF matching network of the 2X mixer. Another version of the front-end is fabricated with the integrated cross-coupled voltage-controlled oscillator. An amplifier has been used to increase the LO input power to the subharmonic mixer. Figure 3.42 shows the block diagram of the receiver front-end. Figure 3.43(a) and Figure 3.43(b) show the die photograph of the integrated receiver front-ends without and with the on-chip oscillator using 0.18 μm SiGe BiCMOS process. The die area of the integrated LNA-subharmonic mixer chip is approximately 2.75 mm \times 1.1 mm. The die area of the integrated LNA-mixer-VCO chip is approximately 3.5 mm \times 1.2 mm.

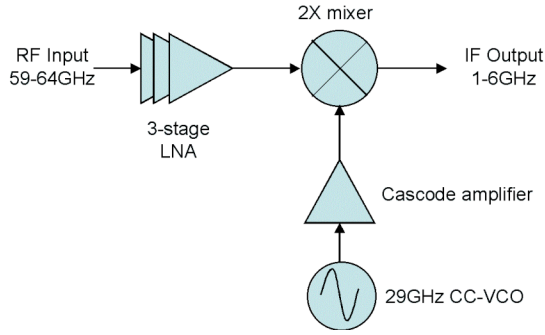


Figure 3.42. Block diagram of subharmonic 60 GHz receiver front-end.

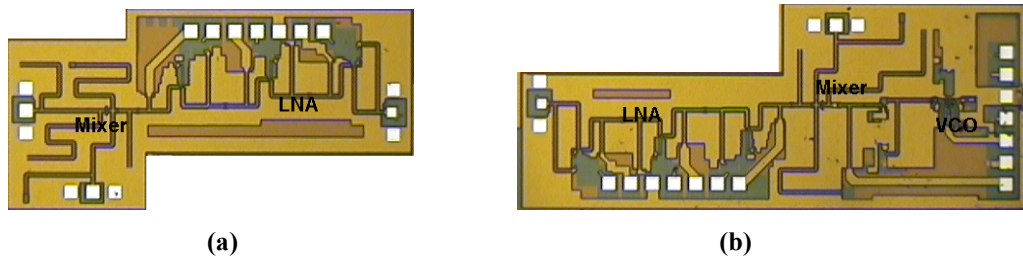


Figure 3.43. (a) Die photograph of the fabricated LNA-subharmonic mixer in 0.18 μm SiGe; (b) Die photograph of the fabricated LNA-subharmonic mixer-VCO in 0.18 μm SiGe.

Measurements have been performed in the integrated receiver front-end chips to determine the conversion gain, bandwidth, and linearity of the LO power. For a 5 dBm, 30 GHz LO signal, the conversion gain of the integrated LNA-mixer is measured to be 16.5 dB for a 2 GHz IF. The total power consumption of this front-end is 27 mW. The LNA consumes this entire power because the passive mixer does not consume any DC power. Figure 3.44 shows the measured conversion gain vs. RF frequency for a 5 dBm, 30 GHz LO (RF power = -50 dBm). Figure 3.45(a) shows the measured conversion gain vs. RF power for 2 GHz IF and 30 GHz, 5 dBm LO. Figure 3.45(b) shows the measured conversion gain vs. LO power for a 2 GHz IF, and -50 dBm, 62 GHz RF. The measured noise figure of the front-end amplifier is approximately 8 dB. Hence, the estimated noise figure of the receiver chain is less than 10 dB.

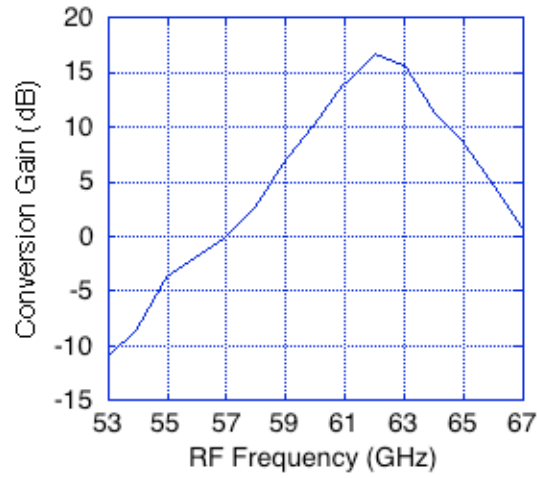


Figure 3.44. Conversion gain of the LNA-mixer vs. RF frequency (30 GHz 5 dBm external LO, -50 dBm RF input power).

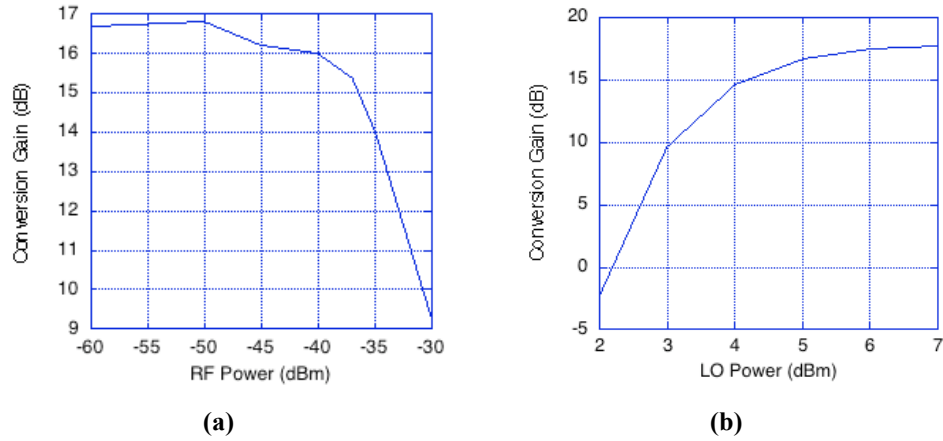


Figure 3.45. (a) Conversion gain of the LNA-mixer vs. RF power (30 GHz 5 dBm external LO, 62 GHz RF); (b) Conversion gain of the LNA-mixer vs. LO power (30 GHz external LO, 62 GHz -50 dBm RF).

The integrated LNA-mixer-VCO module consumes a total of 62 mW (27 mW from LNA, 0 mW from mixer, 20 mW from VCO, and 15 mW from VCO-amplifier). A 15.5 dB conversion gain is achieved for the integrated receiver front-end with the on-chip cross-coupled oscillator. Both the versions realize a RF bandwidth of 4 GHz and approximately -37 dBm of input 1-dB compression point. Figure 3.46(a) shows the

measured conversion gain vs. RF frequency, and Figure 3.46(b) shows the measured conversion gain vs. RF power for the integrated LNA-mixer-VCO.

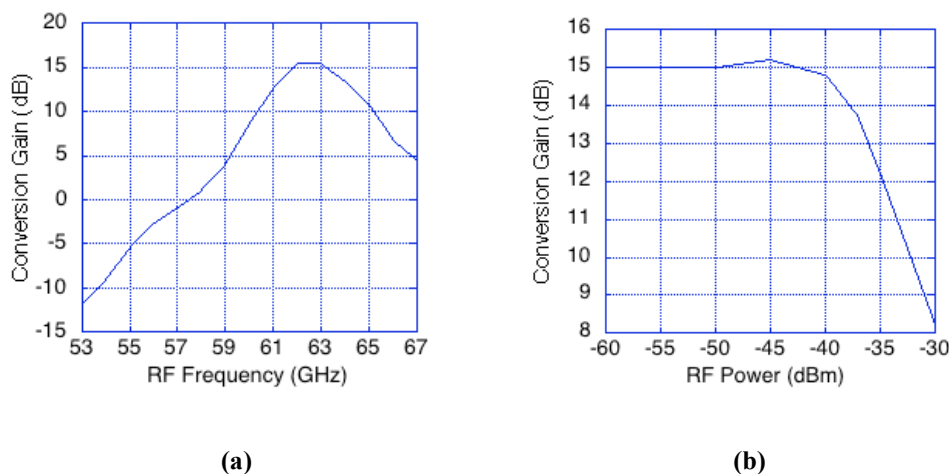


Figure 3.46. (a) Conversion gain of the LNA-mixer-VCO vs. RF frequency (VCO tuned to 30.4 GHz, -50 dBm RF input power); (b) Conversion gain of the LNA-mixer-VCO vs. RF power (VCO tuned to 30.4 GHz, 62 GHz RF).

Measurement results indicate an excellent performance of the 60 GHz subharmonic front-end in low-cost 0.18 μm SiGe. The conversion gain of around 16 dB can be attributed to the high gain of the front-end LNA ($\sim 25\text{dB}$), and low conversion loss of the passive subharmonic mixer ($\sim 9\text{dB}$). The on-chip VCO output power (after the amplifier) can be estimated at around 4.5 dBm from the characteristics of the LNA-mixer with the external LO. This is the first report of a 60 GHz receiver front-end in 0.18 μm SiGe with the comparable performance to high-end IC processes. The front-end is extremely low-power, and can be tuned to heterodyne or direct-conversion architectures with minimal change. This 60 GHz receiver front-end is first reported 60 GHz receiver front-end using 0.18 μm silicon-based IC process.

3.7 Summary

This chapter demonstrates the first 60 GHz receiver front-end implementations in low-cost 0.18 μm SiGe BiCMOS process. In order to realize the receiver front-end, a high-gain cascode amplifier is implemented using a novel gain-boosting technique to overcome the performance limitations of the process.

The first receiver implementation is a non-coherent amplitude-detection scheme integrated with a low-cost organic package. This integrated receiver demonstrates an extremely low power budget of 25 pJ/bit for a multi-gigabit data transmission over the wireless link up to 2 meters of distance. A complete antenna-to-demodulated-baseband solution is integrated in this particular approach. This is the *first report* of a non-coherent 60 GHz receiver front-end integration in 0.18 μm SiGe with the *lowest reported* power budget to date for 60 GHz receivers.

In addition, a subharmonic 60 GHz front-end is also demonstrated *for the first time* using low-cost 0.18 μm SiGe. The front-end provides a conversion gain of 16 dB with 4 GHz RF bandwidth for only 27 mW DC power consumption (62 mW with integrated VCO).

However, the application of such a low-cost low-power SiGe front-end is still limited by the integration of digital baseband processors. A complex true baseband processing (traditionally all CMOS) scheme with multi-Gbps throughput is extremely challenging in a 0.18 μm process. In addition, the amplitude-detection scheme or the subharmonic front-end demonstrated in this chapter cannot scale to a 10 Gbps throughput because of limited front-end bandwidth available (4 GHz instead of full 7 GHz), limitation in terms of application modulation schemes (QPSK realization is extremely challenging in direct-

conversion, and for heterodyne scheme, a high-throughput QPSK would require a IF of at least 6 GHz, i.e., twice the data rate in each channel). Hence, a high-throughput solution requires a better performance IC process suitable for low-cost digital integration, i.e., traditional CMOS. Hence in the next chapter, a 60 GHz heterodyne receiver front-end development is demonstrated using CMOS so that the front-end is suitable for a data rate of 10 Gbps and higher.

Chapter 4

60 GHz Receiver Front-end in CMOS

4.1 Introduction

In this chapter, a heterodyne architecture for the development of 60 GHz receiver front-end, suitable for up to 10-15 Gbps throughput, is demonstrated using a 90 nm CMOS process. The choice of process and architecture is driven by the demand of higher data rate, a scalable architecture, and a dense digital integration. As mentioned in the last chapter, the 60 GHz receiver front-ends implemented using 0.18 μm SiGe cannot be scaled for more than 2-3 Gbps of data throughput. A direct-conversion architecture would be extremely challenging for more complex modulation schemes, i.e., QPSK, QAM, and more complex ones, and hence, the data rate would be limited by the spectral efficiency of the modulation scheme. Again a heterodyne architecture would require an IF at least twice the baseband bandwidth to ensure no aliasing. Hence, assuming 3.5 GHz baseband bandwidth, a 7 GHz or higher IF needs to be selected with 7 GHz of bandwidth; e.g., 3.5 GHz – 10.5 GHz. However, such a heterodyne wideband implementation is extremely challenging for the passive subharmonic front-end implemented in SiGe while maintaining the overall gain of the front-end. On the other hand, an advanced CMOS process could scale the data rate by using spectrally efficient modulation schemes to 10-15 Gbps and more.

In addition, the advantage of digital CMOS lies in its digital integration capabilities. Any advanced radio would need a lot of digital integrated functions, e.g., data recovery, clock recovery, physical device interface (PHY), and media access controller (MAC). Digital baseband processors are traditionally CMOS, and a monolithic integration would require the front-end to be implemented in the same CMOS process.

There have been multiple reports 60 GHz front-end building blocks using 130 nm CMOS process [10], [21], [25], [26]. However, the high noise figure and DC power consumption of the front-end elements using 130 nm CMOS process is not suitable for low-power, ultra-high data rate 60 GHz systems. In addition, multi-Gbps baseband processor would be limited by the performance of 130 nm CMOS process. On the other hand, 60 GHz front-end building blocks developed using 90 nm CMOS process [22]-[24], [52] have a better performance compared to 130 nm CMOS. A significant reduction of the DC power consumption of baseband-processing blocks can also be achieved in 90 nm CMOS process [53]. A receiver front-end gain of approximately 15 dB and an IF-stage gain of 15 dB is targeted with the possibility of variable gain control to satisfy the link-budget requirements and also, to provide approximately -20 dBm power at the output of the IF.

In this chapter, firstly a detailed characterization of the 90 nm CMOS process is described. The characterization includes passive structures, e.g., transmission lines, capacitors, and resistors, single transistors and cascode devices. Next, a systematic design of the two-stage front-end low-noise amplifier is presented. Different down-conversion schemes suitable for the high throughput heterodyne architecture are developed and compared. Different IF amplification blocks are also derived corresponding to different

down-conversion schemes. Finally, a complete 60 GHz receiver front-end is developed for 6.5 GHz- 12.5 GHz IF bandwidth and 23.5 dB conversion gain (30.5 dB voltage gain under loading of second downconversion stage). The complete front-end including the IF-amplifier stages consume only 70 mW DC power, and the front-end is scalable for high spectral-efficiency modulation schemes, i.e., up to 10-15 Gbps of data throughput. Another version of the 60 GHz front-end is investigated that provides around 34 dB voltage gain at the input of the second downconversion mixer. This is the first complete report of a 60 GHz CMOS receiver front-end from the antenna to the IF suitable for up to 10-15 Gbps of data throughput.

4.2 Characterization of 90 nm CMOS process

The characterization of the 90 nm CMOS process is necessary [10] because of the unavailability of the accurate device models and transmission line models. The s-parameter measurement results have been measured and extracted using off-wafer LRRM calibration with ABCD matrix deembedding of *thru* device as mentioned in chapter 3.2. Figure 4.1 shows the photograph of the *thru* device. Figure 4.2(a) and Figure 4.2(b) show the measured s-parameters of the *thru* for two different chips. The bondpad portion of the *half-thru* is coplanar waveguide in nature because of the ground plane in two sides. The feeding portion of the *half-thru* is microstrip in nature with $50\ \Omega$ characteristics impedance and ground plane at the bottommost metal layer. The deembedding and extraction process is summarized below:

- i. VNA calibration using off-wafer ISS;
- ii. Measurement of the *thru*
- iii. Measurement of the DUT
- iv. Extraction of *feeding* ABCD matrix from *thru* ABCD matrix
- v. Extraction of DUT ABCD matrix by deembedding

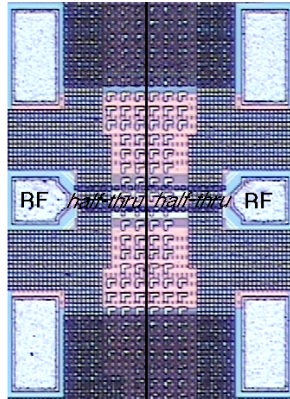


Figure 4.1. Die photograph of the fabricated *thru* structure in 90 nm CMOS.

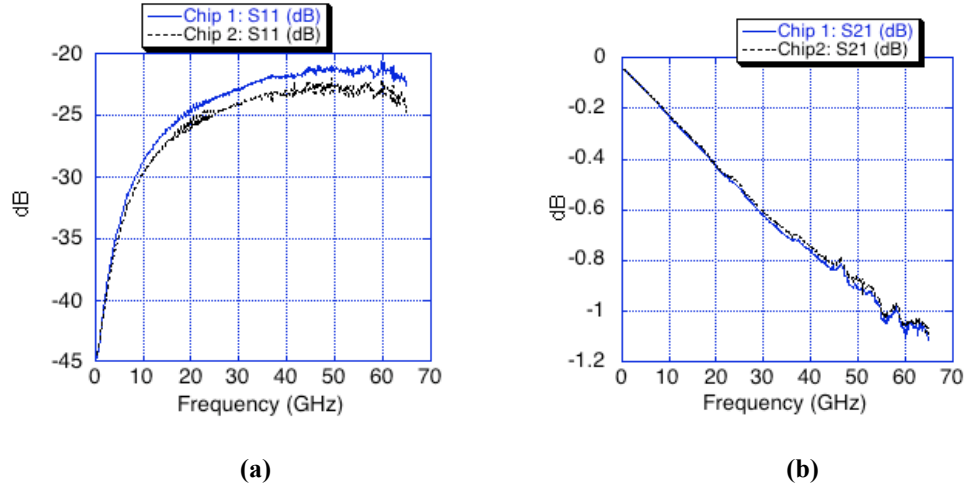


Figure 4.2. (a) Measured return loss of the *thru* device; (b) Measured insertion loss of the *thru* device.

4.2.1 Characterization of passive devices in 90 nm CMOS process

The choice of the topology of the transmission line is very significant because the matching networks at 60 GHz would consist of transmission lines. In CMOS, 50 Ω transmission lines are usually more lossy than SiGe or GaAs substrates [10] because of less thick signal metal layer, very thin dielectric layer, and also the low-K material used as the dielectric material. The 0.9 μm thick top metal layer is chosen as the signal layer. Both coplanar-waveguide and microstrip transmission lines are fabricated to determine the suitable option. The CB-CPW alternative is ruled out because side-ground planes along with a close bottom-ground plane would require a narrow 50 Ω transmission line, and resistive losses would increase. The width of the microstrip 50 Ω transmission line is 8 μm , the width of the CPW transmission line is chosen as 8 μm at 3 μm distance with side-ground planes. Figure 4.3 and Figure 4.4 show measurement results of these transmission lines.

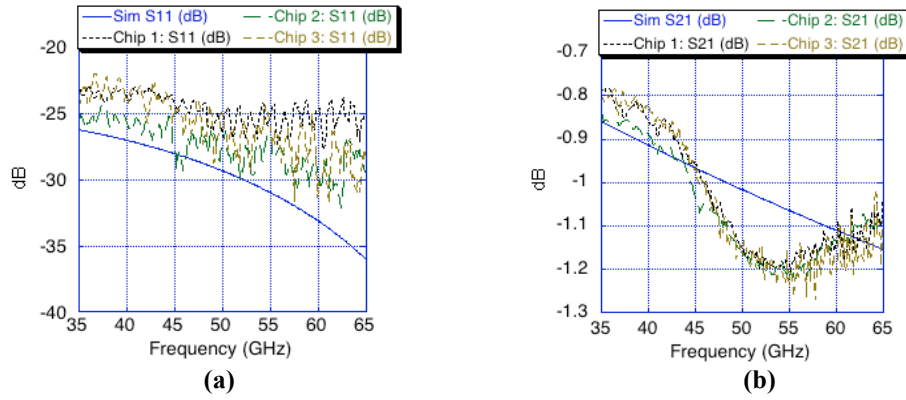


Figure 4.3. (a) Measured and modeled return loss of the 1 mm microstrip transmission line; (b) Measured and modeled insertion loss of the 1 mm microstrip transmission line.

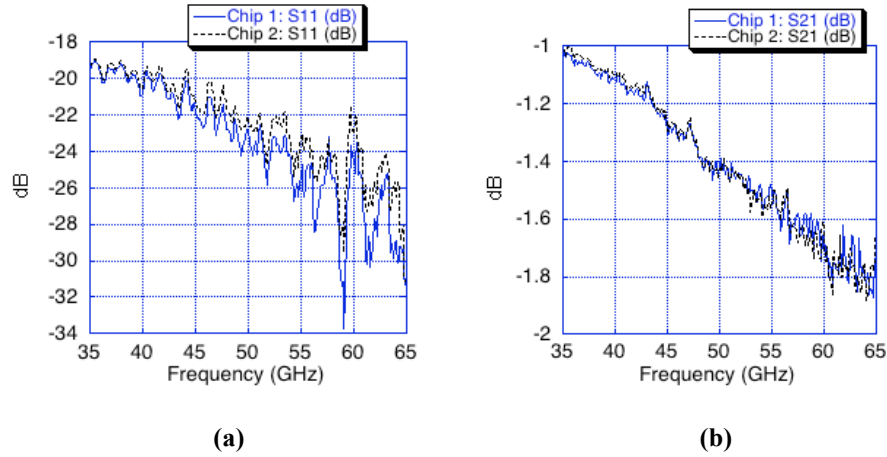


Figure 4.4. (a) Measured return loss of the 1 mm CPW transmission line; (b) Measured insertion loss of the 1 mm CPW transmission line.

Measurement results show a better performance of the microstrip transmission line compared to the CPW transmission line. Hence, the microstrip configuration has been chosen for the circuit implementation. A scalable model in terms of the length of the 8 μm wide microstrip transmission line is developed. Another microstrip line of 600 μm length has been added to verify the correlation between the simulation model and measurements. The simulated model and measurement results correlate well with each other as shown in Figure 4.5. The measured phase also have less than 2 % variation compared to the model.

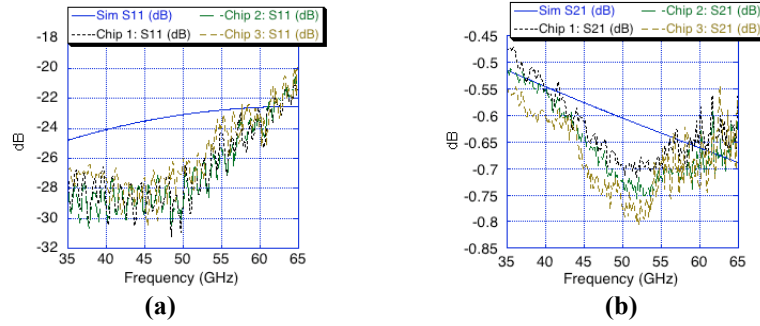


Figure 4.5. (a) Measured and modeled return loss of the 600 μm microstrip transmission line; (b) Measured and modeled insertion loss of the 600 μm microstrip transmission line.

A 240 fF MIM capacitor is measured to develop a model with an equivalent series plate inductance. The capacitor dielectric is 15 μm wide and 8 μm long. Figure 4.6 shows the measured and modeled capacitance (with series inductances accounting for plate inductances).

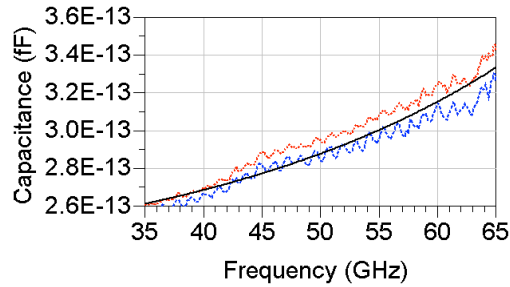


Figure 4.6. Measured and modeled results of 240 fF MIM capacitance.

In addition, a 50 Ω silicided poly resistor is also characterized. The silicided poly resistors have minimum parasitic capacitance, and hence, can be useful for high-frequency circuit designs. Figure 4.7 shows the measured resistance, and the resistor can be used at high frequencies due to very small parasitic capacitance.

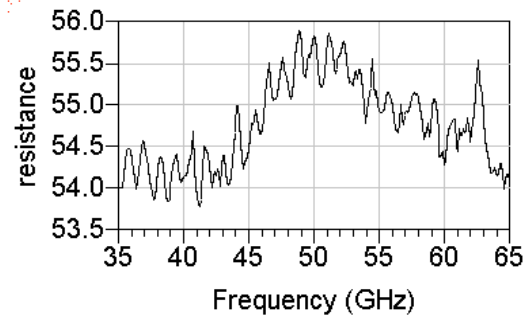


Figure 4.7. Measured resistance vs. frequency of the 50 Ω silicided poly resistor.

4.2.2 Characterization of active devices in 90 nm CMOS process

Different single-transistor devices and cascode devices are measured to characterize them. The finger size of transistors is chosen as 1 μm to increase the f_{max} [10]. Figure 4.8 shows the schematic of the single-transistor and cascode test structures.

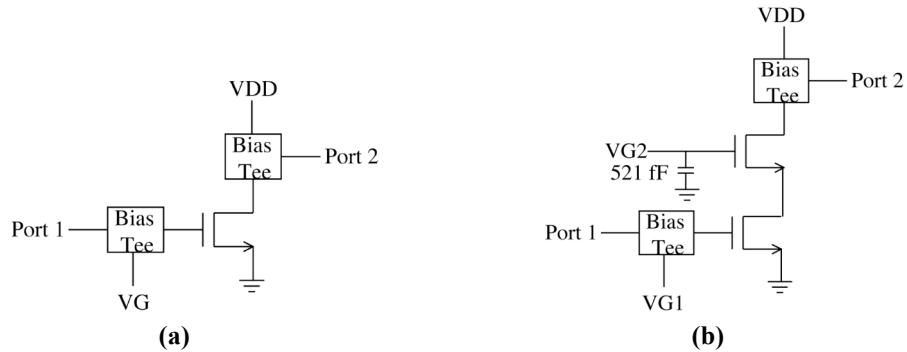


Figure 4.8. (a) Schematic of the single NMOS test structure; (b) Schematic of the cascode NMOS test structure.

A set of single-device and cascode test structures is fabricated. Figure 4.9 shows the DC measurement results for the 40 μm wide and 60 μm wide device. Figure 4.10 shows the s-parameter measurement results of the 40 μm wide NMOS device ($V_G = 0.6$ V, $V_{DD} = 1$ V). Figure 4.11 shows the s-parameter measurement results of the 60 μm wide NMOS device ($V_G = 0.6$ V, $V_{DD} = 1$ V). Figure 4.12 shows the maximum available gain (MAG) of 40 μm wide and 60 μm wide devices.

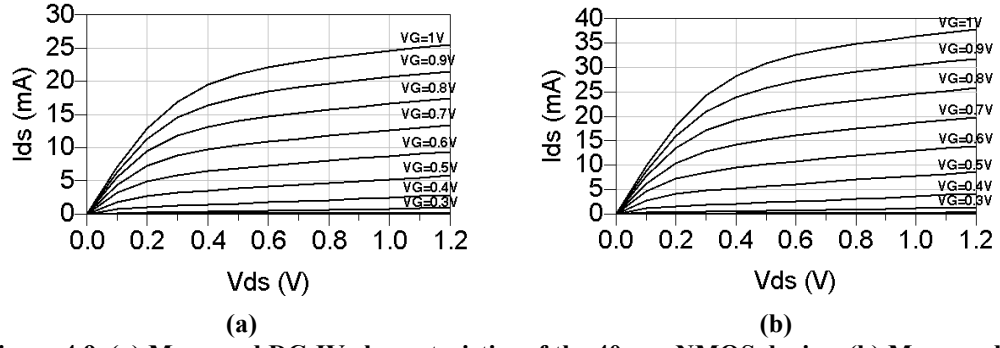


Figure 4.9. (a) Measured DC-IV characteristics of the 40 μm NMOS device; (b) Measured DC-IV characteristics of the 60 μm NMOS device.

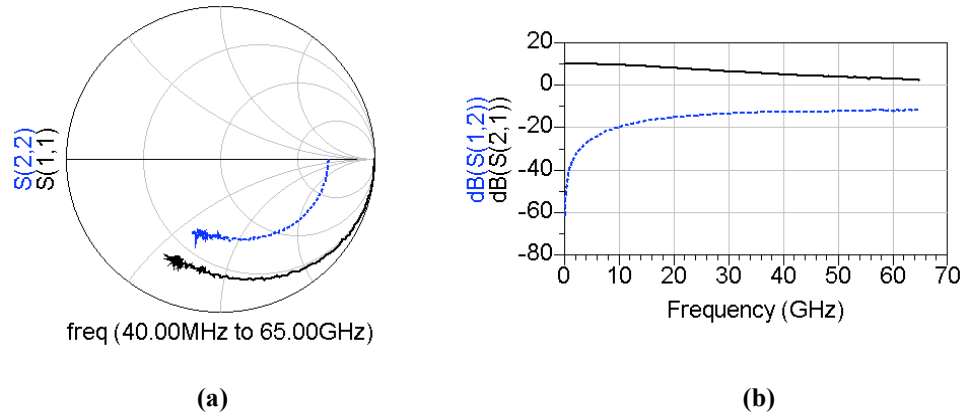


Figure 4.10. (a) Measured S_{11} and S_{22} of the 40 μm NMOS (gate bias = 0.6 V, drain bias = 1 V); (b) Measured S_{21} and S_{12} of the 40 μm NMOS (gate bias = 0.6 V, drain bias = 1 V).

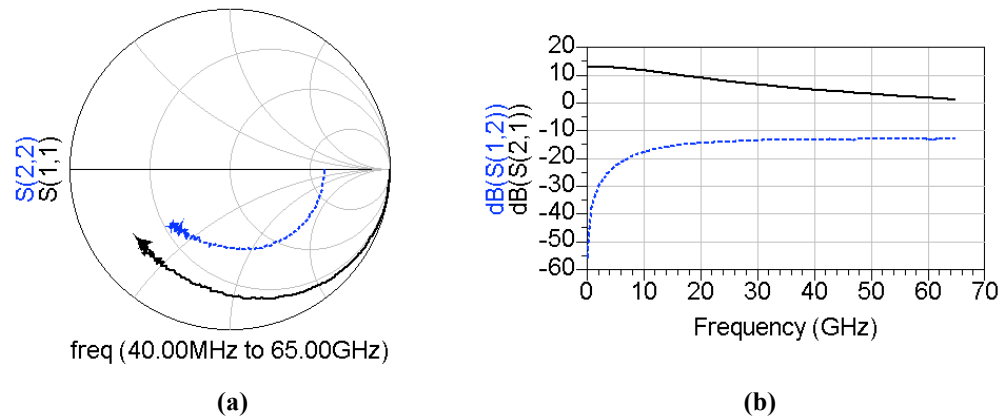


Figure 4.11. (a) Measured S_{11} and S_{22} of the 60 μm NMOS (gate bias = 0.6 V, drain bias = 1 V); (b) Measured S_{21} and S_{12} of the 60 μm NMOS (gate bias = 0.6 V, drain bias = 1 V).

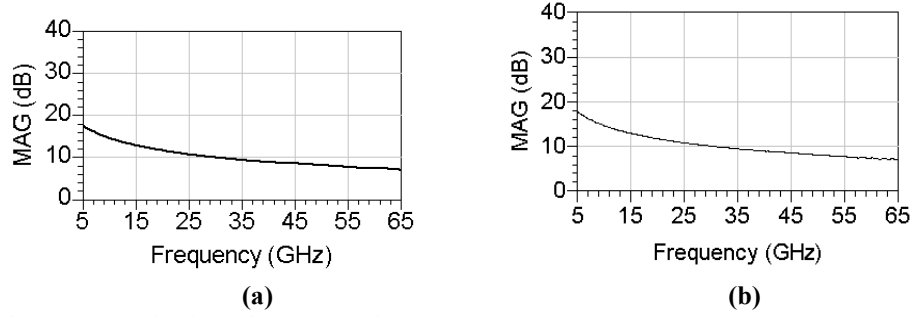


Figure 4.12. (a) MAG of the 40 μm NMOS (gate bias = 0.6 V, drain bias = 1V); (b) MAG of the 60 μm NMOS (gate bias = 0.6 V, drain bias = 1V).

From Figure 4.12, the 40 μm wide device has similar MAG at 55 GHz – 65 GHz compared to the 60 μm wide device. However, the 60 μm wide device would consume approximately 50 % higher current for obtaining that maximum gain. In addition, the noise performance of the 40 μm wide device would be good enough for 60 GHz applications [10]. Hence, the 40 μm wide is chosen as the input device for the 60 GHz front-end low-noise amplifier. The measured f_T of the 40 μm wide device is higher than 115 GHz, and the measured f_{max} is higher than 180 GHz. A cascode topology is chosen because of higher gain at a lower DC power consumption with a decent noise performance [10], [22]. Two different cascode devices are fabricated; (a) with 40 μm wide CS device and 40 μm wide CG device, and (b) with 40 μm wide CS device and 60 μm wide CG device. Figure 4.13 shows measured s-parameters of the first cascode device ($V_{G1} = 0.6$ V, $V_{G2} = 1.5$ V, $V_{DD} = 1.8$ V). Figure 4.14 shows measured s-parameters of the second cascode device ($V_{G1} = 0.6$ V, $V_{G2} = 1.5$ V, $V_{DD} = 1.8$ V).

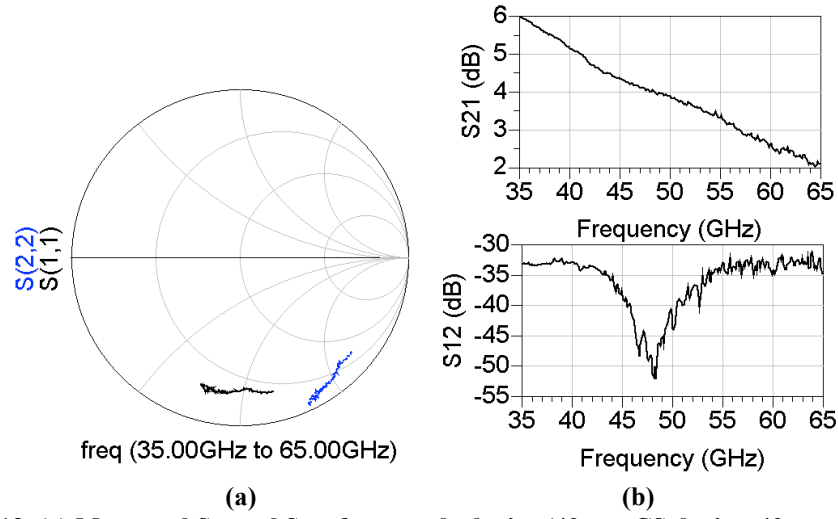


Figure 4.13. (a) Measured S_{11} and S_{22} of a cascode device (40 μm CS device, 40 μm CG device); (b) Measured S_{21} and S_{12} of a cascode device (40 μm CS device, 40 μm CG device).

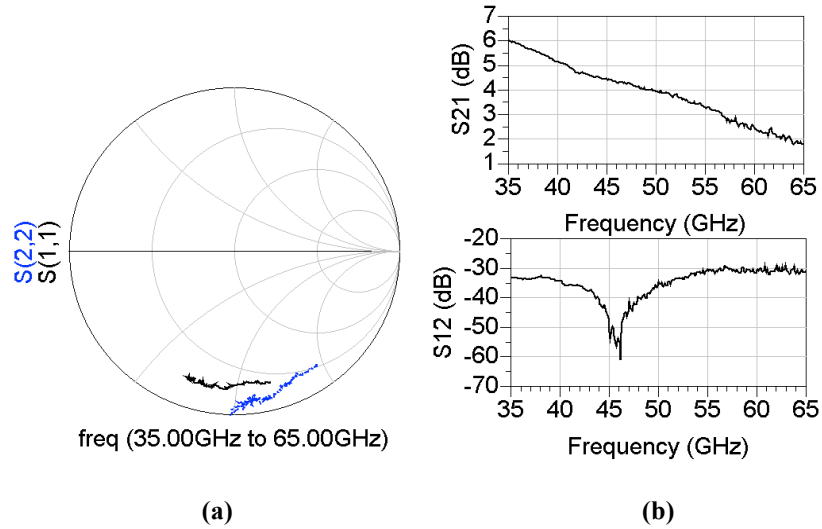


Figure 4.14. (a) Measured S_{11} and S_{22} of a cascode device (40 μm CS device, 60 μm CG device); (b) Measured S_{21} and S_{12} of a cascode device (40 μm CS device, 60 μm CG device).

Both cascode devices draw similar DC current (~ 8 mA) under the given operating condition. However, the downslope of S_{21} is higher in case of the second cascode structure (40 μm CS device, 60 μm CG device) as compared to the first cascode structure (40 μm CS device, 40 μm CG device). This is because of a higher capacitance in the cascode node in case of the second cascode structure with a larger CG device. Hence, we choose the 40 μm CS device and the 40 μm CG device in the cascode structure for the

front-end low-noise amplifier. The design of the low-noise amplifier is described in the next sub-chapter.

4.3 Development of 60 GHz CMOS low-noise amplifier

The front-end low-noise amplifier is the most critical block in terms of the receiver sensitivity and DC power consumption. A cascode structure with both 40 μm devices has been chosen as the amplifier core.

4.3.1 Development of CMOS 60 GHz single-stage low-noise amplifier

Measured s-parameters of the cascode core have been used in the development of the single-stage prototype of CMOS 60 GHz low-noise amplifier. The scalable 8 μm wide transmission line model is used to design the input-matching and output-matching networks. A nominal current consumption of 0.2 mA/ μm has been chosen as a trade-off between gain, noise figure, and DC power consumption. The basic schematic of the low-noise amplifier core is shown in Figure 4.15.

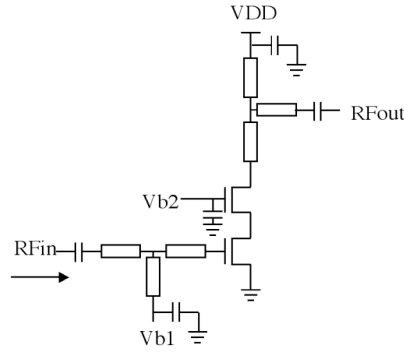


Figure 4.15. Basic schematic of the 60 GHz CMOS cascode amplifier.

Stubs in the input-matching and output-matching networks are used to provide DC gate bias and drain bias respectively. These stubs are shorted with 900 fF MIM capacitors in input and output-matching networks. However, one very important phenomenon is observed in terms of the low-frequency response of the amplifier. The gate bias is assumed to go through a 5 K Ω series resistance so that it behaves as an open circuit

parallel to the shorting capacitor. Four different cases are investigated as follows: (a) Open circuit (ideal DC feed) after the 900 fF on-chip shorting capacitor for drain bias, (b) a 300 pH inductor to large shorting capacitor to feed VDD after the 900 fF on-chip shorting capacitor for drain bias (similar to bondwire inductance), (c) a 6 nH inductor to large shorting capacitor to feed VDD after the 900 fF on-chip shorting capacitor (similar to the inductance of a typical DC probe), and (d) a perfect short instead of the 900 fF shorting capacitor. Figure 4.16 depicts simulated s-parameters corresponding to these four cases.

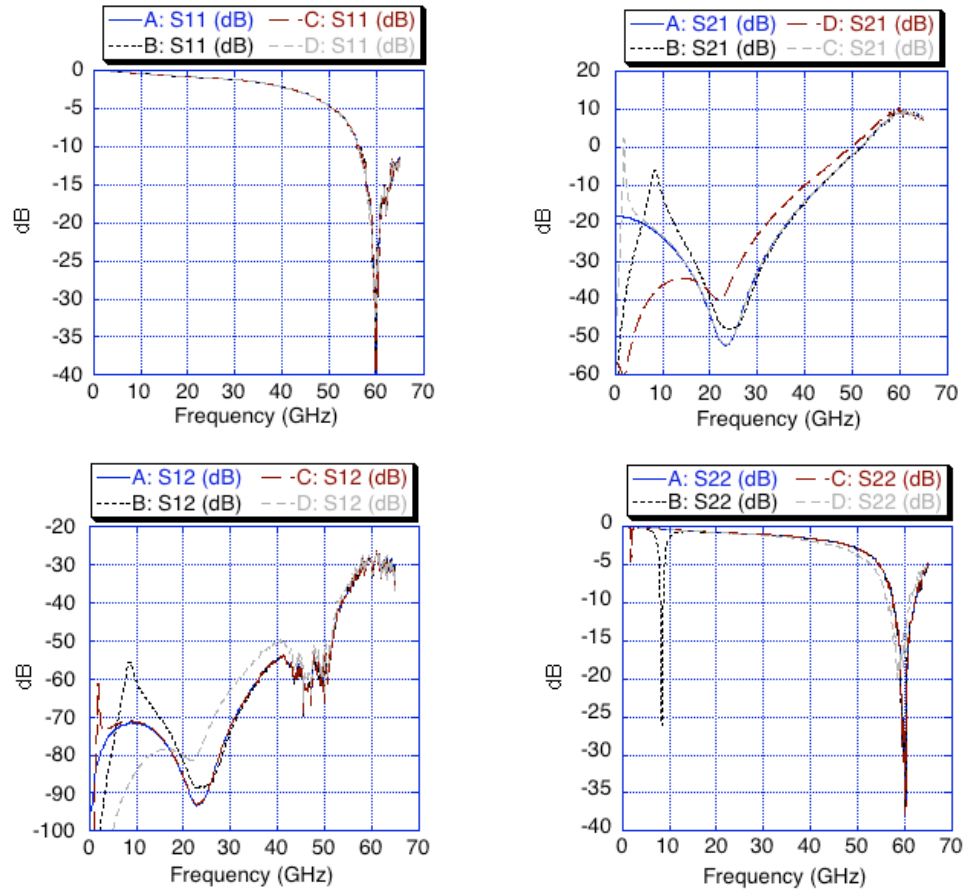


Figure 4.16. Simulated s-parameters of the single-stage 60 GHz cascode amplifier corresponding to four different DC-feed alternatives.

Simulated results show an oscillation tendency at a much lower frequency without a proper short at the stub of the output-matching network. In reality, it is not possible to implement a perfect short at the end of the stub. Hence, an additional RC network (with small R) is added just after the 900 fF shunting capacitor. In case of an integrated front-end, multiple MIM capacitors would be required as decoupling capacitors on the VDD line to prevent any low-frequency oscillation tendency. Figure 4.17 shows the complete schematic of the implemented one-stage low-noise amplifier. No bends are used in transmission lines to reduce uncertainties. Another 3 pF MIM decoupling capacitor is connected to the VDD pad. Figure 4.18 shows the die photograph of the single-stage 60 GHz low-noise amplifier fabricated using 90 nm CMOS. The amplifier occupies an area of 1.07 mm \times 0.66 mm.

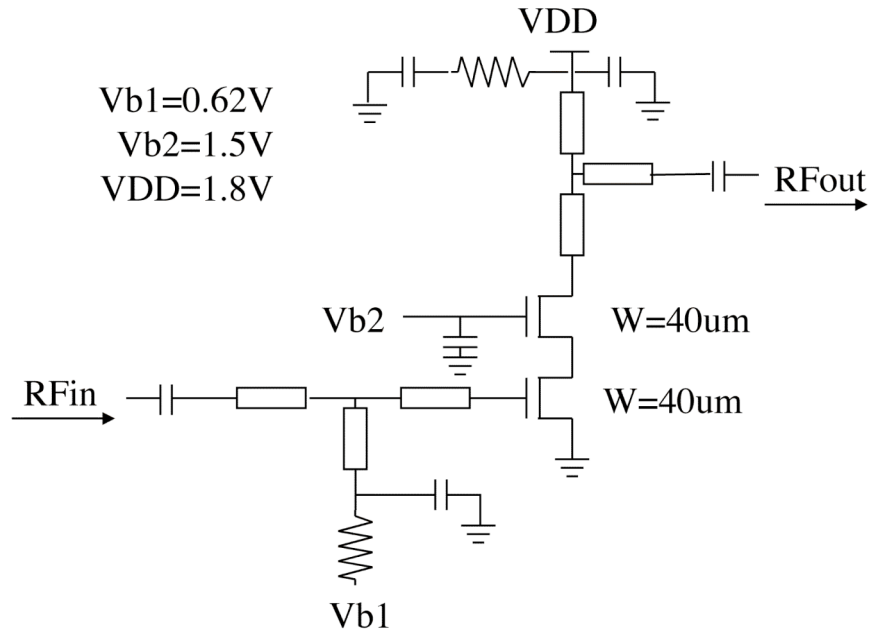


Figure 4.17. Schematic of the one-stage 60 GHz low-noise amplifier with nominal bias conditions.

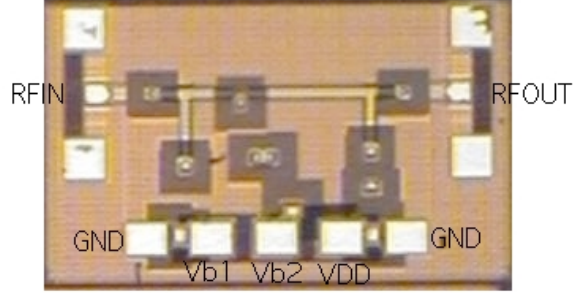


Figure 4.18. Die photograph of the one-stage 60 GHz low-noise amplifier using 90 nm CMOS.

Measurement results show a maximum power gain of approximately 7 dB for a DC power consumption of 14.5 mW, i.e., 8.1 mA from 1.8 V supply. The measured output P1 dB is approximately 1 dBm. The 1-dB bandwidth is larger than 6.5 GHz, i.e., 58.5 GHz – (>) 65 GHz. The measured noise figure is approximately 6 dB at 60 GHz. Figure 4.19 shows measured and simulated s-parameters of the amplifier.

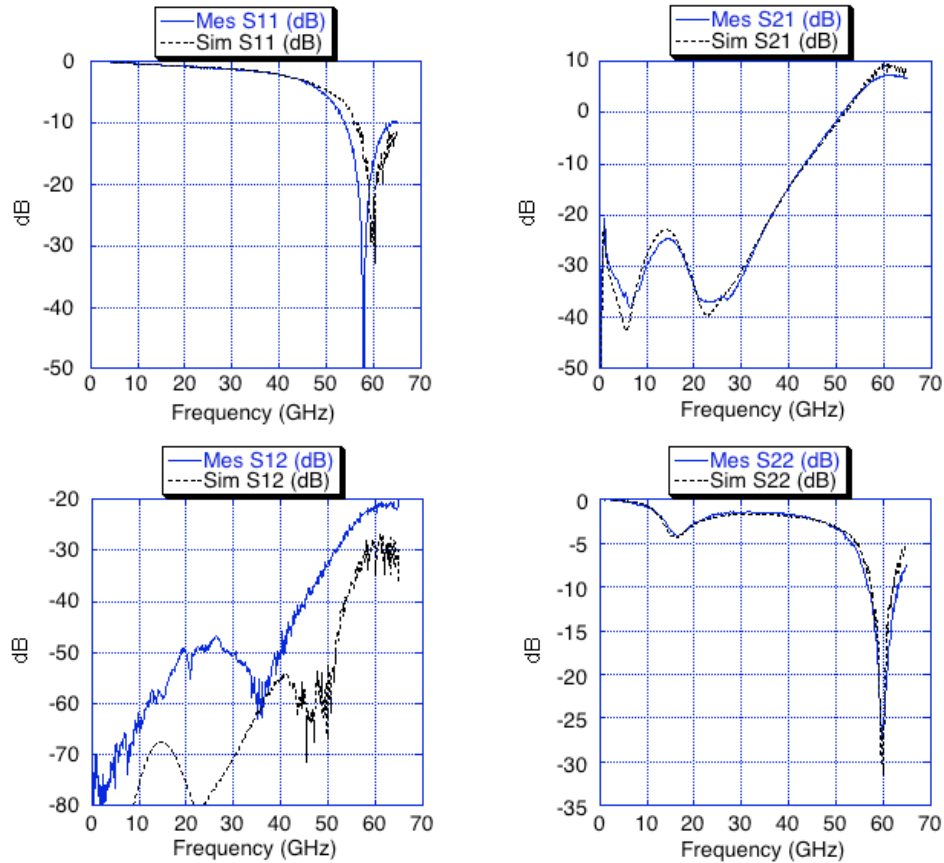


Figure 4.19. Simulated and measured s-parameters of the 60 GHz CMOS amplifier.

Simulated s-parameters match well with measured s-parameters in the 60 GHz frequency range and low frequencies. The low-frequency oscillation tendency can be suppressed more by using more decoupling capacitors in integrated receiver front-ends.

4.3.2 Development of CMOS 60 GHz front-end low-noise amplifier

To satisfy the gain specifications of the typical heterodyne 60 GHz front-end, approximately 15 dB front-end amplifier gain is targeted. Approximately 0 dB of conversion gain can be expected from the down-conversion mixer [26]. Hence, a two-stage cascode amplifier can serve the purpose of the 60 GHz front-end low-noise amplifier.

The schematic of the front-end amplifier is shown in Figure 4.20 along with typical bias requirements. Additional decoupling MIM capacitors have been placed on DC-bias pads. Figure 4.21 shows the die photograph of the fabricated 60 GHz front-end low-noise amplifier.

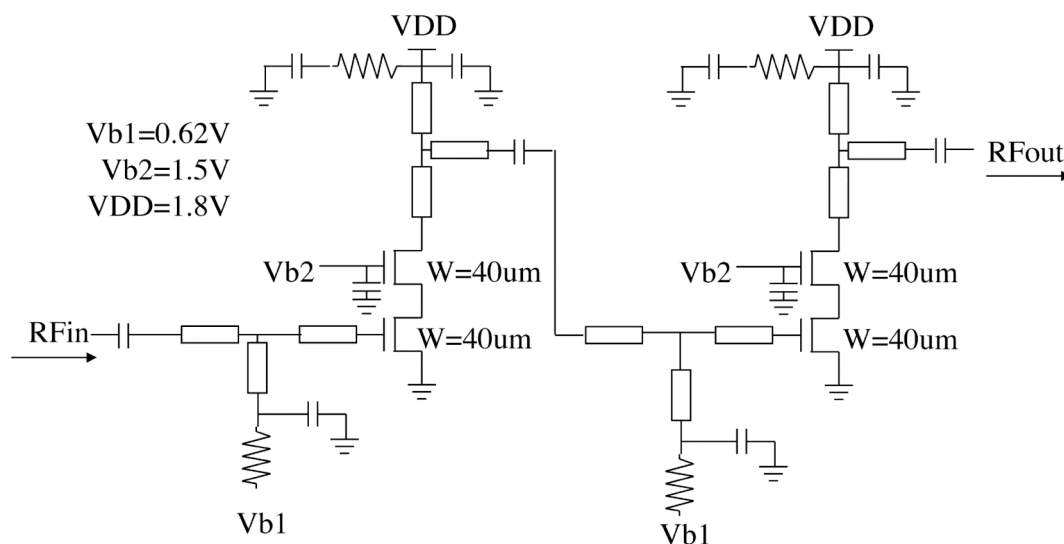


Figure 4.20. Schematic of the 60 GHz CMOS front-end low-noise amplifier.

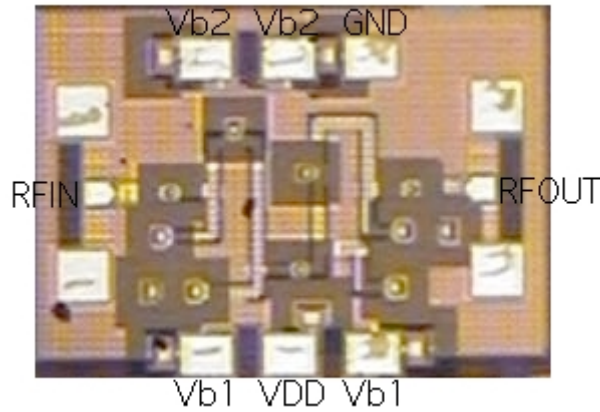


Figure 4.21. Die photo of the fabricated 60 GHz CMOS front-end low-noise amplifier.

The front-end amplifier occupies an area of $0.91 \text{ mm} \times 0.66 \text{ mm}$ with the pads. The amplifier core occupies only $0.45 \text{ mm} \times 0.4 \text{ mm}$. Such a compact implementation is possible by using transmission line bends. The transmission-line-based matching networks are characterized using EM-simulation tools, e.g., IE3D and momentum. It is possible to reduce the area even more by having close bends in transmission lines.

Measurement results indicate 15.5 dB gain with excellent input and output matching of the amplifier at 60 GHz. The 1-dB bandwidth is 59.3 GHz-65 GHz. The front-end amplifier consumes only 16.4 mA from 1.8 V power supply. The measured noise figure is approximately 6-7 dB in the frequency band. The measured output P1 dB is 1 dBm. Figure 4.22 shows measured s-parameters of the front-end amplifier. Figure 4.23 shows the measured noise figure of the amplifier. Figure 4.24 demonstrates the variation of the gain with the increasing input power at 62 GHz.

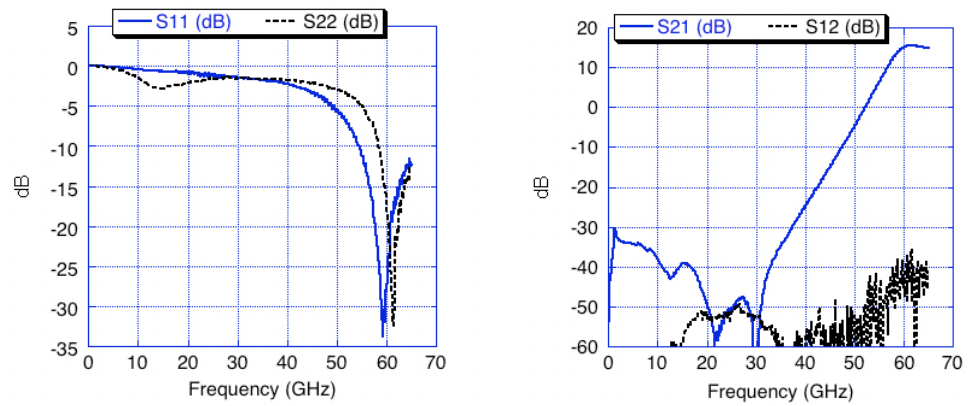


Figure 4.22. Measured s-parameters of the 60 GHz CMOS front-end low-noise amplifier.

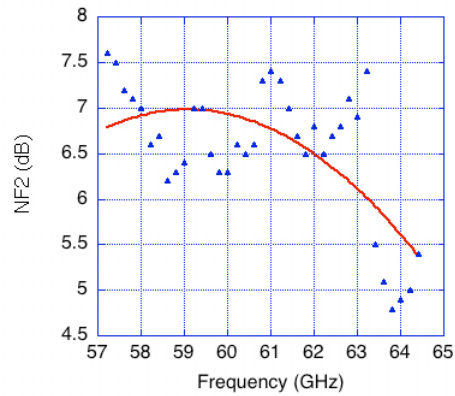


Figure 4.23. Measured noise figure of the 60 GHz CMOS front-end low-noise amplifier.

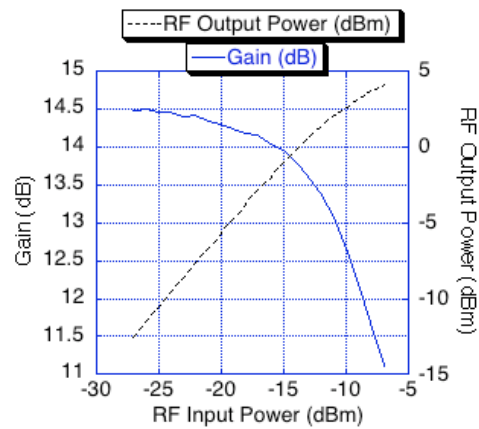


Figure 4.24. Gain and output power of the front-end amplifier with increasing input power at 62 GHz.

Table 4.1 compares the front-end LNA with other reported silicon-based 60 GHz LNAs. This particular CMOS implementation demonstrates the highest gain among the CMOS LNAs with the very accurate and wideband frequency characteristics.

Table 4.1. Comparison of silicon-based 60 GHz LNAs.						
Process [Ref]	Topology	Frequency (GHz)	Gain (dB)	Noise Figure (dB)	DC Power (mW)	Output P1dB (dBm)
0.12 μm SiGe HBT[20]	1-stage CG + caoscocode	56-64	15	4.5	11	-5@ 61 GHz
0.13 μm CMOS [21]	3-stage cascode	51-57	>20	~8	72	1.8@ 56 GHz
0.13 μm CMOS [10]	3-stage cascode	51-65	12	8.8	54	2@ 60 GHz
90nm CMOS [22]	2-stage cascode	55-60	14.6	5.5	24	-0.5@ 58 GHz
90nm CMOS [23]	2-stage CS	NA	12	6	10.4	4 @60 GHz
0.18 μm SiGe [3 rd chapter] [27]	3-stage cascode [modified]	58-63	24	7.9 @60 GHz	25	-5@ 60 GHz
90 nm CMOS [This work]	2-stage cascode	57-(>) 65 59.3- 65 1-dB BW	15.5	6 @ 60 Ghz	29	1 @60 GHz

Another version of the front-end amplifier has been designed with 60 μm CS and 60 μm CG devices. This version has not been fabricated separately. This LNA has been integrated with a single-balanced Gilbertcell mixer to characterize the complete front-end. However, this particular version of the front-end has been designed relying upon simulation models of the design kit, and hence, a downshift in frequency is observed during measurement. This front-end LNA uses similar input and output-matching networks. The detailed schematic and measurement results have been provided in Chapter 4.5.

4.4 Development of 60 GHz CMOS down-conversion mixer

Two different alternatives are investigated to develop an efficient down-conversion scheme in 90 nm CMOS. The first version is a double-gate mixer. Figure 4.25(a) shows the schematic of the double-gate mixer core. The second alternative is the single-balanced Gilbertcell mixer. Figure 4.25(b) shows the schematic of the Gilbertcell core.

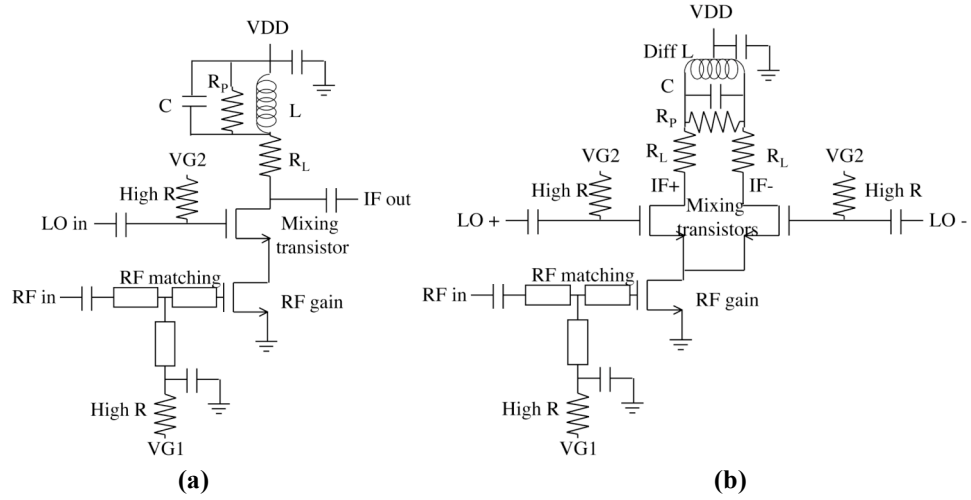


Figure 4.25. (a) Schematic of the double-gate mixer core; (b) Schematic of the single-balanced Gilbertcell core.

A double-balanced structure has not been implemented because of large interconnect parasitics associated with the cross-coupled connection in the mixer. The LO leakage suppression is targeted in the subsequent IF amplifier stages using rejection stubs at LO frequency.

In both mixer architectures, there is a direct trade-off between the size of the CS device (for RF gain) and mixing transistors. A high g_m is required from the CS device to obtain a higher RF gain; i.e., a stronger RF signal to the source of the mixing transistor(s). Hence, a large current consumption is required. On the other hand, the mixing efficiency increases when the mixing transistors are biased at the threshold (a

much lower DC bias current). A current bleeding technique is utilized at lower frequencies to provide the additional DC current to the CS device only through another bypass path, and the bypass path should present very high impedance to the RF/LO signals. Such an implementation is reported in [18] using 130 nm CMOS process. However, the current-bleeding technique increases the overall current consumption and the die area of the mixer, and may not be required in the advanced 90 nm CMOS process with the focus being a low-power implementation.

The CS device width is chosen as 40 μm to obtain a higher transconductance at a lower power consumption. The V_{DS} of the CG device is kept much higher compared to that of the CS device, to reduce the V_{GS} of the CG device as compared to that of the CS device. This is required for a higher mixing efficiency. For the Gilbertcell mixer, the width of mixing transistors can be one-half of the size of the CG device in the double-gate mixer to keep a similar parasitic capacitance at the common node so that the input impedance does not change.

The double-gate mixer, in principle, requires a higher LO power and provides a less conversion gain (or more conversion loss) as compared to the Gilbertcell mixer due to the full-cycle mixing efficiency of the Gilbertcell mixer. However, the Gilbertcell mixer requires a differential LO input signal.

The load of two mixers are inductive peaking loads to increase the IF bandwidth of the down-conversion. The targeted IF bandwidth is 6 GHz - 12 GHz for the RF frequencies within the unlicensed 57 GHz – 64 GHz band. The series resistance R_L provides necessary resistive drop to bias the mixing transistor(s) efficiently, and also to provide the gain at lower IF frequencies. The capacitor C provides bandpass

characteristics required to cut-off LO leakage through the mixer. The loading of the IF amplifier and transmission-line interconnects need to be considered while designing the bandpass load. Mixers are implemented together with the LNA and the IF amplifier/buffer stage separately to study the system characteristics. The measurement-system impedance is $50\ \Omega$, and hence it reduces the gain of the system as compared to the standard capacitive load for the second down-conversion mixer. The performance of these CMOS heterodyne 60 GHz front-ends, suitable for a scalable 10 – 15 Gbps wireless data transmission, has been presented in the next sub-chapter.

A different version of the Gilbertcell mixer is also implemented with a resistive load targeting a lower IF frequency (3 GHz -7 GHz). The mixer is integrated with the two-stage LNA and an IF buffer (to provide unity voltage gain and required power gain for $50\ \Omega$ measurement system). A frequency downshift is noted because the design has been done using insufficient simulation models. The performance of this integration is described in the next sub-chapter.

4.5 Integrated CMOS 60 GHz receiver Front-end

The integrated CMOS 60 GHz receiver front-end is presented in this sub-chapter. Three different variations of the front-ends have been demonstrated. The first version integrates a two-stage LNA with the single-balanced Gilbertcell mixer with resistive load targeting a lower IF frequency (4 GHz IF bandwidth). An on-chip balun is used to generate the differential LO signal from the single-ended LO input. An output buffer is present at the IF output to convert the output impedance to 50 Ω .

The second integrated front-end version integrates a two-stage LNA with a double-gate mixer and a three-stage IF amplifier. A LO-rejection stub is present in the IF amplifier stage to reduce the LO leakage signal. A single-ended to differential converter is used as the second stage of the IF amplifier because the final IF output needs to be differential in nature. It is measured to have a 23.5 dB conversion gain over an IF bandwidth of 6.5 GHz – 12.5 GHz for 51 GHz LO with only 70 mW DC power consumption. The IF output is not 50 Ω , and it can account for 7-8 dB lower gain as compared to the capacitive load of the second down-conversion mixer.

A third integration option is investigated with a Gilbertcell mixer and a three-stage IF amplifier. This prototype is investigated as a part of the integrated 60 GHz receiver development. Hence, a separate characterization is not possible for the front-end. However, an expected performance on the basis of the performance of the building blocks is presented. A 34 dB conversion gain is expected with 4 GHz – 12 GHz IF bandwidth for 53 GHz LO with only 82 mW DC power consumption.

4.5.1 Integrated CMOS 60 GHz receiver front-end (version 1)

This version has been designed using simulation models of the 90 nm design kit. Hence, a frequency shift is noticed. This integrated receiver consists of a two-stage LNA, a Gilbertcell mixer, and an IF buffer with 50 Ω output impedance. The LNA has a cascode core with 60 μm wide CS and CG device. The CS device of the Gilbertcell is 30 μm wide, and mixing transistors are 20 μm wide. Figure 4.26 shows the schematic of the integrated front-end.

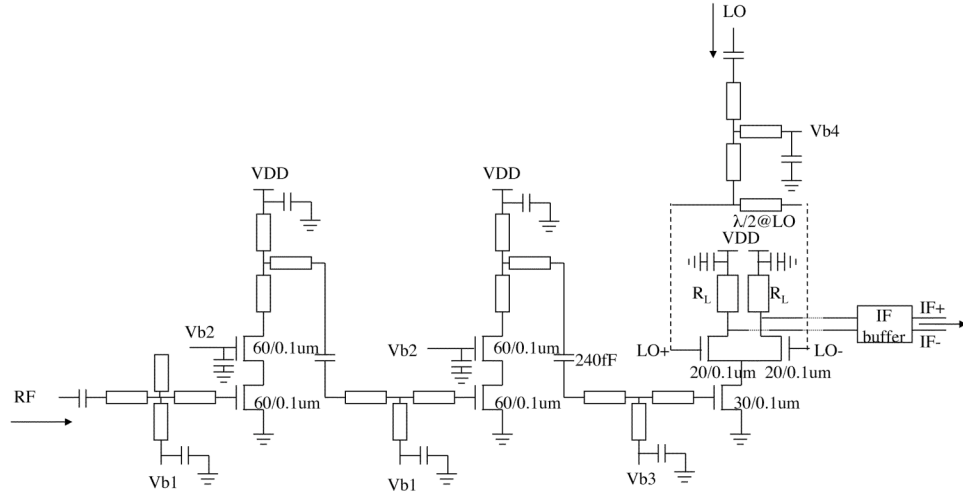


Figure 4.26. Schematic of the integrated 60 GHz receiver front-end (version 1).

The IF buffer provides unity voltage gain at 50 Ω output impedance. An on-chip LO matching network is followed by a simple balun utilizing a $\lambda/2$ transmission line at LO frequency. An IF of 3 GHz – 8 GHz is targeted in this particular application, and hence, a resistive mixer loading is sufficient. The series DC-block capacitor (~ 1 pF) generates a high-pass characteristics, and this characteristics coupled with the low-pass characteristics of the mixer generates a bandpass response of IF. Figure 4.27 shows the

die photo of the fabricated LNA-Mixer. It occupies an area of 2 mm × 1.25 mm (the effective die area is less than 50 % of the total die area).

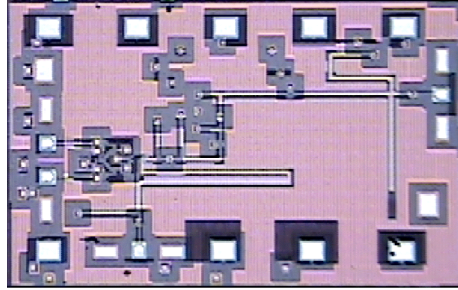


Figure 4.27. Die photograph of the integrated 60 GHz receiver front-end (version 1).

The characterization of the LNA-Mixer chip requires a test board that has been designed and fabricated. The LNA-Mixer has been assembled in the test board as shown in Figure 4.28. All the DC bias is provided through the test board.

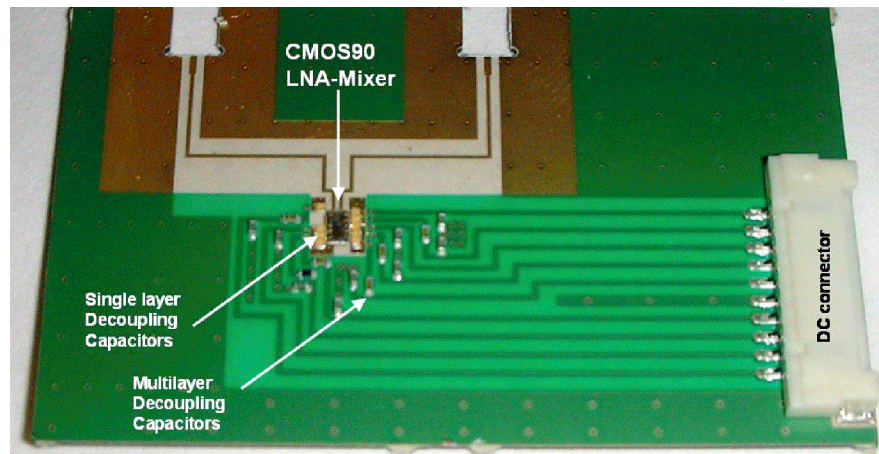


Figure 4.28. Photograph of the LNA-Mixer chip mounted on the test board.

Measurement results of the LNA-mixer show around 17 dB conversion gain with 3 GHz-7 GHz 3-dB IF bandwidth for a LO of 53 GHz with -2 dBm power (an expected -4 dBm differential LO power at Gilbertcell input). Different measured performance parameters are shown in Figures 4.29-4.33. Table 4.2 summarizes the performance parameters.

Table 4.2. Measured performance of the LNA-Mixer.	
Conversion Gain	17 dB
IF bandwidth	3 GHz – 7 GHz
RF bandwidth	56 GHz – 60 GHz
Noise Figure	8 dB
DC power consumption	52 mW (44 mW from LNA + 8 mW from mixer)
RF matching	> 10 dB at 50 GHz – 56.5 GHz
LO matching	> 10 dB at 46 GHz – 53.5 GHz
Input P1 dB	- 23 dBm
LO power	-2 dBm single-ended @ 53GHz

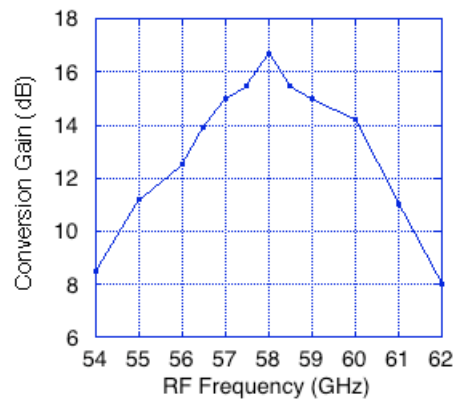


Figure 4.29. Measured conversion gain vs RF frequency (LO frequency = 53 GHz, LO power = - 2 dBm).

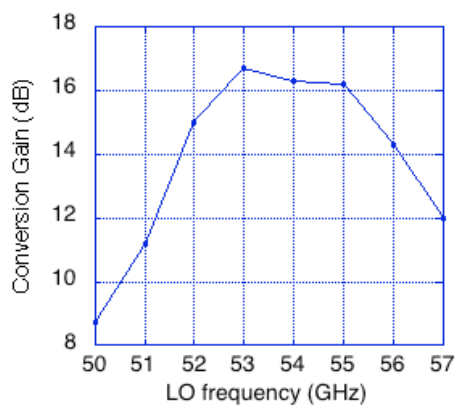


Figure 4.30. Measured conversion gain vs LO frequency (IF frequency = 5 GHz, LO power = -2 dBm).

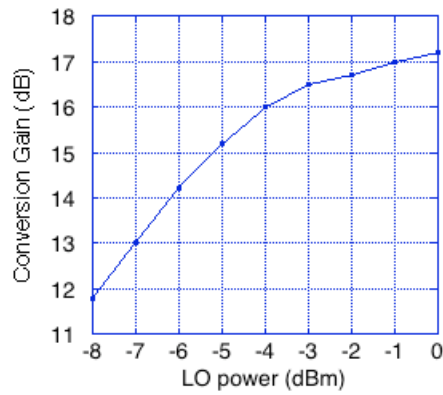


Figure 4.31. Measured conversion gain vs LO power (RF frequency = 58 GHz, LO frequency = 53 GHz).

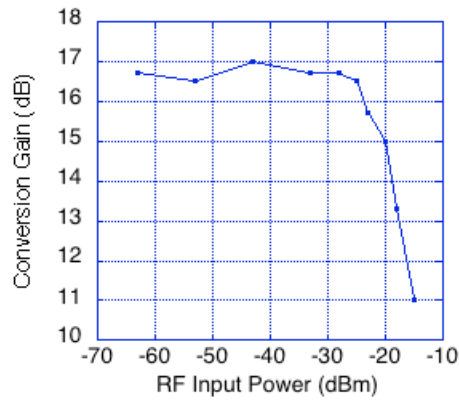


Figure 4.32. Measured conversion gain vs RF power (RF frequency = 58 GHz, LO frequency = 53 GHz, LO power = -2 dBm).

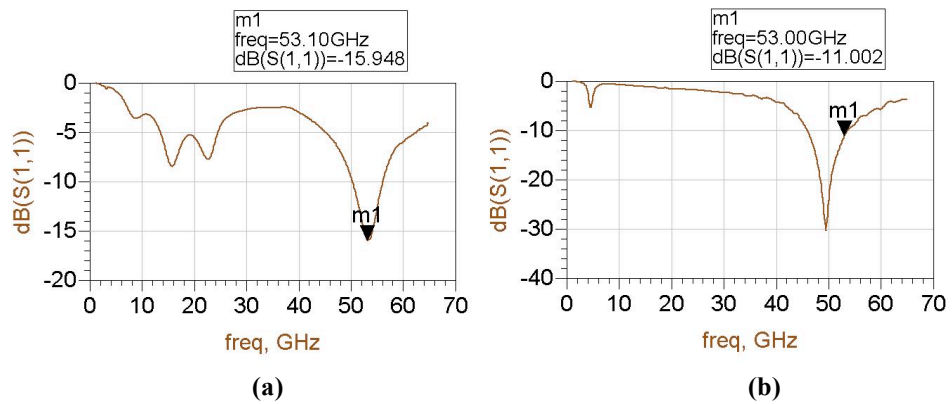


Figure 4.33. (a) Measured RF-port matching; (b) Measured LO-port matching.

This integrated LNA-Mixer presents an excellent potential in terms of a heterodyne 60 GHz CMOS front-end receiver. This potential is exploited in full in the subsequent sub-chapters.

4.5.2 Integrated CMOS 60 GHz receiver front-end (version 2)

This integrated receiver includes a two-stage LNA (optimized using measured s -parameters of cascode core), a double-gate mixer (suitable for the single-ended LO), and three-stage IF amplifier. There is no impedance matching from the output of the mixer as only voltage gain is considered. The first stage of the IF amplifier is a cascode amplifier with a LO-rejection stub at the drain of the common source transistor. The load is inductive peaking in nature. The output of the first stage goes to a single-ended-to-differential converter. The last stage is a differential amplifier that reduces the amplitude imbalance of the differential signal generated by the single-ended-to-differential converter. Loads of the second and the third stages are also of inductive peaking nature. The third amplifier stage is directly loaded by $50\ \Omega$ during the measurement using the spectrum analyzer. That $50\ \Omega$ comes in parallel with the inductive load of the third stage. Hence, the measured gain is reduced by 7-8 dB as compared to the loading of the baseband mixer, i.e., $40\ \mu\text{m}$ wide NMOS transistor. Also, the capacitance of the output-bondpad has not been considered in the design, and this capacitance reduces the gain and bandwidth to a small extent. This capacitive effect would not be present in case of integrated second down-conversion mixer.

Figure 4.34 shows the schematic of the integrated 60 GHz CMOS heterodyne receiver using double-gate mixing. This front-end is suitable for an IF bandwidth of 6 GHz – 12 GHz. This IF bandwidth translates into a 6 Gbps data rate for QPSK, and 12

Gbps for QAM modulation schemes. Figure 4.35 shows the die photo of the fabricated integrated receiver front-end. The front-end occupies an area of $1.25 \text{ mm} \times 1.25 \text{ mm}$.

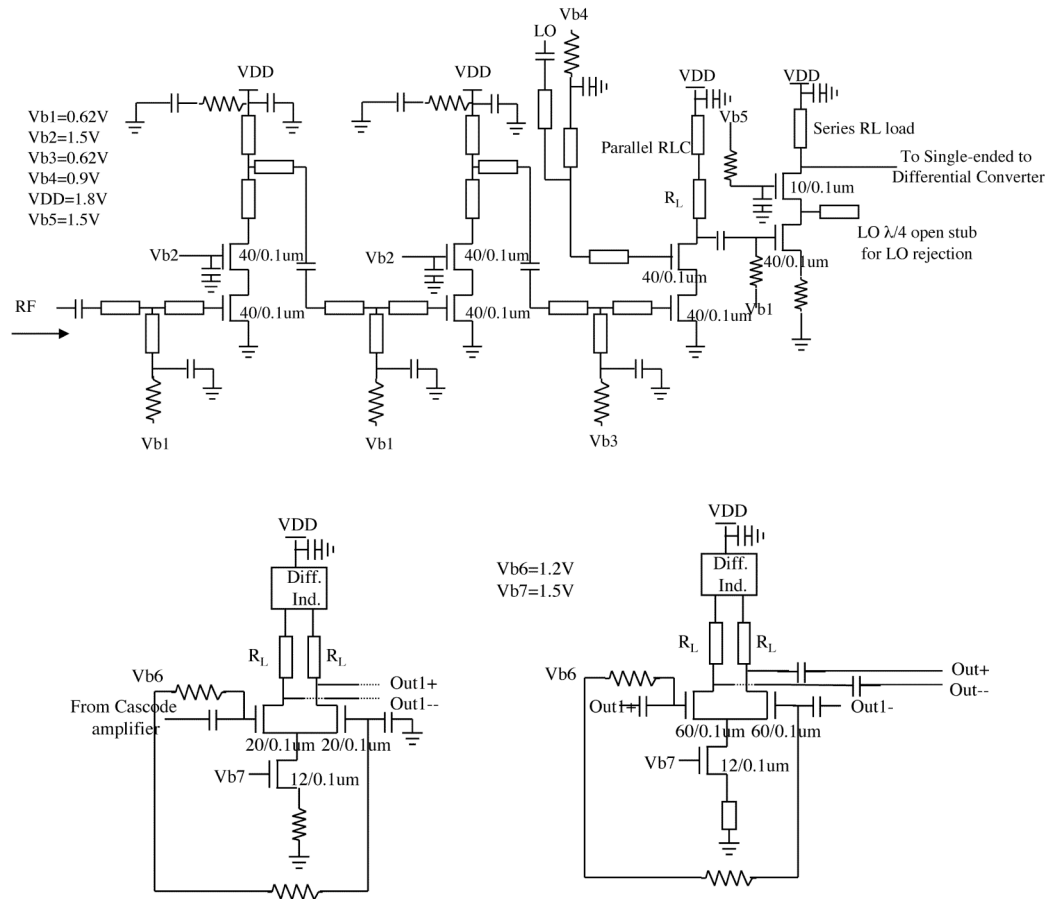


Figure 4.34. Schematic of the integrated 60 GHz CMOS heterodyne front-end (two-stage LNA + double gate mixer + three-stage IF amplifier).

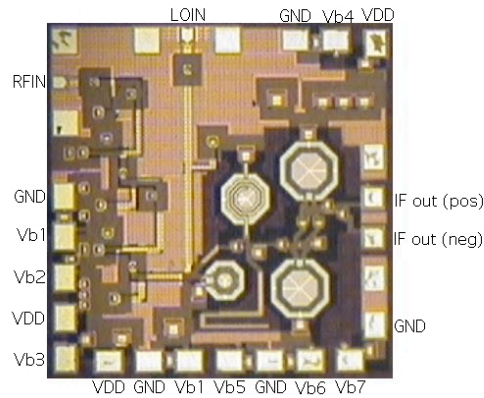


Figure 4.35. Die photograph of the integrated 60 GHz CMOS heterodyne front-end (version 2).

The characterization of the receiver front-end chip requires a test board that has been designed and fabricated. The receiver front-end has been assembled in the test board as shown in Figure 4.36. All the DC bias is provided through the test board.

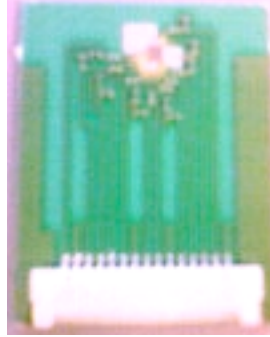


Figure 4.36. Photograph of the test board to measure the receiver front-end chip.

Measurement results show a conversion gain of 23.5 dB (deembedded to 30.5 dB in case of capacitive loading) with a 6.5 GHz – 12.5 GHz of IF bandwidth at 51 GHz LO frequency; i.e., a RF bandwidth of 57 GHz – 63 GHz. The total DC power consumption is only 70 mW. The measured output P1 dB is 0 dBm. The LO leakage is less than –33 dBm (differential). The amplitude imbalance for the differential output is less than 0.3 dBm. The expected noise figure is less than 8 dB. These measurement results indicate an excellent performance of the 60 GHz heterodyne receiver front-end in 90 nm CMOS suitable for 10-15 Gbps of wireless data transmission.

Figures 4.37-4.40 shows different performance parameters of the receiver front-end. Table 4.3 summarizes the performance of the receiver front-end.

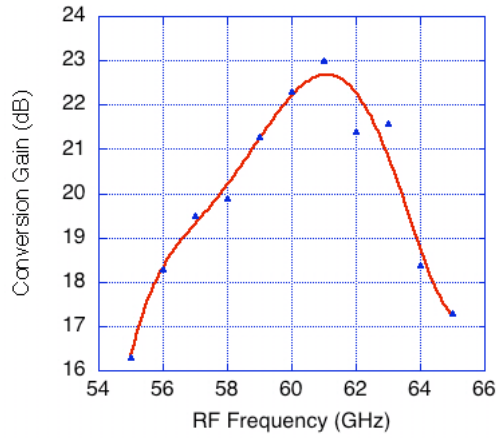


Figure 4.37. Conversion gain of the LNA-Mixer-IFamp with RF frequency (RF power = -34 dBm, LO frequency = 51 GHz, LO power = -2 dBm).

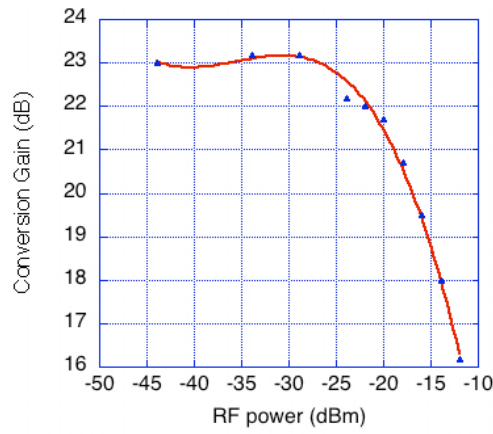


Figure 4.38. Conversion gain of the LNA-Mixer-IFamp with RF power (RF frequency = 61 GHz, LO frequency = 51 GHz, LO power = -2 dBm).

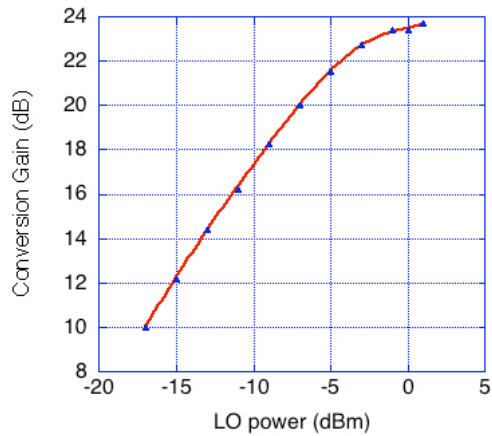


Figure 4.39. Conversion gain of the LNA-Mixer-IFamp with LO power (RF frequency = 61 GHz, LO frequency = 51 GHz, RF power = -34 dBm).

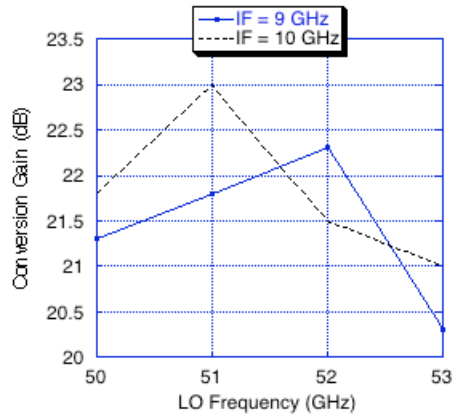


Figure 4.40. Conversion gain of the LNA-Mixer-IFamp with LO frequency (LO power = -2 dBm, RF power = -34 dBm).

Table 4.3. Performance of the integrated receiver front-end (version 2).		
Performance Measure	Measured	Simulated
Gain	23.5 dB (30.5 – 31.5 dB in case of capacitive loading with 40 μ m wide NMOS)	26.5 dB (34.5 dB in case of capacitive loading with 40 μ m wide NMOS)
3-dB BW	57.5 GHz – 63.5 GHz	57 GHz – 64 GHz
Output P1 dB	0 dBm	1 dBm
DC power consumption	70 mW (38 mA from 1.8 V supply)	75 mW (41.5 mA from 1.8 V supply)

The 3-dB gain reduction is mostly due to approximately 2.5 dB gain reduction in the two-stage LNA as seen previously. This gain reduction can be compensated using a higher supply voltage. The measured conversion gain increases by 2 dB for a 0.2 V increase in supply voltage.

4.5.3 Integrated CMOS 60 GHz receiver front-end (version 3)

The third version of the integrated receiver front-end integrates a two-stage LNA with a single-balanced Gilbertcell mixer and a three-stage IF amplifier. The differential IF output of the Gilbertcell mixer is fed into two cascode amplifiers with LO rejection stubs at drains of CS transistors. Outputs of cascode amplifiers are fed into two differential amplifier stages, and the final stage would see the input impedance of the second down-conversion mixer as the load impedance. It would typically be a 40 μm wide NMOS transistor. This version of the front-end is investigated for the integration with the baseband circuits, and hence a separate characterization is not performed. Figure 4.41 shows the block diagram of the receiver front-end. Table 4.4 summarizes the performance of the front-end.

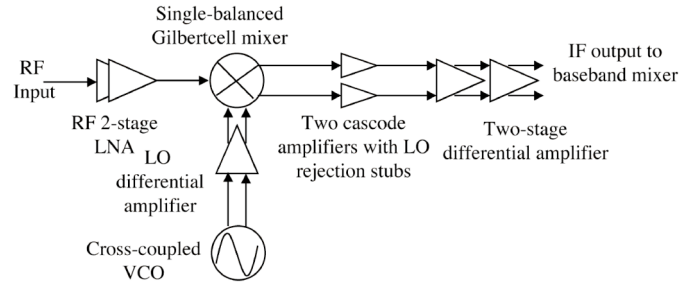


Figure 4.41. Schematic of the integrated receiver front-end utilizing Gilbertcell mixing.

Table 4.4. Performance of the integrated receiver front-end (version 3).	
Conversion Gain	34 dB
RF Bandwidth	57 GHz – 65 GHz
IF Bandwidth	4 GHz – 12 GHz
Noise Figure	8 dB
DC Power consumption	82 mW (two-stage LNA + Gilbertcell mixer + three-stage IF amplifier)
Output P1 dB	2 dBm
LO power requirement	-4 dBm differential @53 GHz

4.6 Summary

This chapter demonstrates the implementation of 60 GHz heterodyne receiver front-end using 90 nm CMOS process. Different versions of the front-end are investigated and implemented to be able to support up to 10-15 Gbps of data rate depending on the baseband modulation scheme. A front-end gain of 23.5 dB (30.5 dB for capacitive loading of the second down-conversion mixer) is demonstrated for an IF bandwidth of 6.5 GHz – 12.5 GHz, i.e., a RF bandwidth of 57.5 GHz – 63.5 GHz, for only 70 mW of DC power consumption. A modified version of the front-end provides 34 dB gain for 4 GHz – 12 GHz IF bandwidth. These are the most wideband demonstrations of the receiver front-end in CMOS processes.

In order to develop the receiver front-end, a systematic characterization of both passive and active devices are performed in the 90 nm CMOS process. A front-end two-stage LNA is developed cascading two cascode amplifier stages. The LNA provides 15.5 dB gain for a DC power consumption of 29 mW. The 1-dB bandwidth is 59.3 GHz – 65 GHz. The measured noise figure is approximately 6-7 dB in the entire frequency band. The measured output P1 dB is 1 dBm. The front-end LNA demonstrates the highest-gain with a very accurate and wideband frequency characteristics among the reported 60 GHz CMOS LNAs.

Two different types of mixers are implemented to accommodate different heterodyne solutions. The LO rejection is implemented in the subsequent IF stages for both the mixers. A double-gate mixer is implemented with a single-ended LO power requirement of –2 dBm. The IF output of the double-gate mixer is single-ended. Hence, an IF single-ended-to-differential converter is required to generate a differential IF output. On the

other hand, a single-ended Gilbertcell mixer is implemented with approximately -4 dBm differential LO power requirement. Different versions of integrated front-end are developed with these two versions of the down-conversion mixer.

The complete CMOS 60 GHz receiver front-end is extremely critical in terms of the single-chip 60 GHz transceiver integration. The baseband signal processor and digital processors are essentially CMOS, and easily be integrated with the front-end into a compact solution. In addition, low-cost packaging techniques demonstrated in the third chapter, and also for the preparation of test boards for CMOS receiver front-ends, opens the potential of very low-cost, ultra high-speed 60 GHz wireless communication applications.

Chapter 5

Millimeter-wave Multi-band and Tunable Circuit Development

5.1 Introduction

In this chapter, the development of different building blocks, suitable for millimeter-wave multi-band applications, is illustrated. Today, wireless communication is witnessing tremendous growth with the proliferation of various standards covering wide, local, and personal area networks (WAN, LAN, and PAN) that operate at different data rates at multiple frequency bands. In the future, the same trend would be translated into millimeter-wave frequencies. In this chapter, a passive directional filter-based multiplexer and a frequency-tunable amplifier is demonstrated as the proof-of-concept for millimeter-wave multi-band building blocks. The directional-filter structure is studied in detail to develop a systematic design procedure for compact directional filters [54]. Two diplexers with 4 GHz and 8 GHz band separation are designed around 40 GHz utilizing the directional-filter structure. A system-on-package (SOP) solution is investigated for millimeter-wave multi-band module.

In the next section, a frequency-tunable amplifier development is described using phase-tunable transmission lines in a multi-metal-layer silicon process. The amplifier frequency response shifts by 7 GHz around 30 GHz under different control conditions. The amplifier also provides a balanced gain in each of the frequency bands. This tunable

amplifier demonstrates the potential of tunable elements for multi-band and cognitive wireless modules.

5.2 Millimeter-wave directional filter and multiplexer development

In this section, a systematic design and analysis procedure towards the successful implementation of 3D LTCC multilayer-loop directional filters and multiplexers at millimeter-wave frequencies is presented. The multilayer low-temperature co-fired ceramic (LTCC) substrates offer excellent passive integration capability for the SOP-module development [14], [55]. Microstrip implementations are preferred in a system of low complexity and easy integrability. Microstrip multilayer-loop directional filters have been investigated in C band [56]. Also, transmission line coupling has been utilized in [57] for lower microwave frequencies. Multiplexing capabilities of the cascaded directional filter system has been shown in [58] at lower RF frequencies. However, there has been no previous report of such implementations at millimeter-wave frequencies. The design rule limitations of LTCC process (unlike thin-film processes) drive us to utilize multilayer technology and vertical coupling to enable actual 3-D integration at millimeter-wave frequencies.

5.2.1 Design and optimization of directional filters

5.2.1.1 Theoretical limitations for planar realization

Different directional filter structures include waveguide cavity filters, strip resonator filters and traveling wave loop filters. Realization of the waveguide structures on LTCC requires lots of vias. Loop resonator filters occupy less area compared to half or full wavelength strip resonator filters. Hence, we focus on microstrip single loop resonator directional filters in our subsequent discussion that can be extended to the possible multi-loop structures. Fractional bandwidth specifications have been determined as

approximately 5% in order to satisfy the bandwidth requirements of high data rate millimeter-wave systems.

The LTCC process provides a multilayer design platform with 100 μm dielectric thickness per layer and a dielectric constant of 5.4. Design rules allow minimum metal width and spacing of approximately 75 μm .

Figure 5.1 shows the simplest microstrip or stripline 50 Ω implementation of the single loop directional filter. At the frequency of operation, the signal couples to the loop resonator. Each side of the resonator is $\lambda_g/4$ long at bandpass frequency, so that the complete loop is λ_g long. The bandwidth depends on the coupling coefficient between the loop and feeding transmission lines.

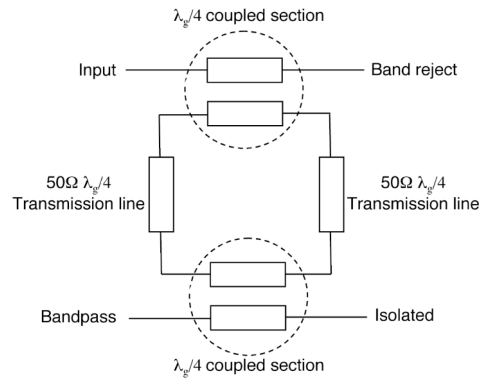


Figure 5.1. Schematic of the four-port microstrip loop directional filter.

Firstly, we study the case of the edge-coupled structures for the directional filter implementation. Figure 5.2 shows the relation between the fractional bandwidth and the theoretical even mode characteristic impedance in a 50 Ω environment, and the required spacing (for different number of dielectric layers between microstrip signal layer and ground layer in the given LTCC process) to achieve the required even-mode impedance for an edge-coupled section.

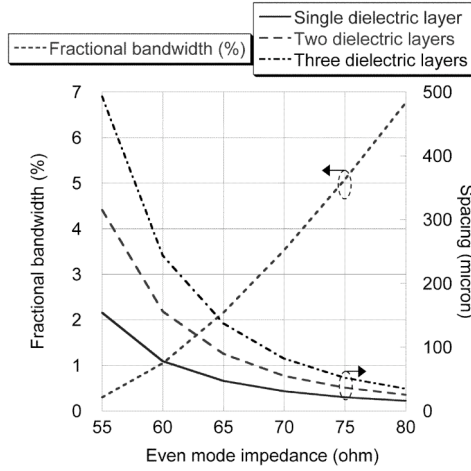


Figure 5.2. Theoretical variation of the fractional bandwidth with the even-mode impedance and the corresponding spacing of the edge-coupled section.

Hence an even-mode impedance of around 75Ω is required to obtain a fractional bandwidth of approximately 5 %. That requires around $50 \mu\text{m}$ spacing even for three dielectric layers between signal and ground layers. In reality, if we consider the difference in the effective dielectric constants for the even and the odd modes, we would require even higher even-mode impedance and a smaller spacing between the edge-coupled transmission lines. Also, increasing the number of dielectric layers will increase the loss in a microstrip implementation. Consequently, the planar realization of microstrip loop directional filters is not possible following the given design rules.

5.2.1.2 Vertical-coupling implementation

In this section, we consider the vertical coupling between the input transmission line and embedded loop resonator to realize the directional filter. Also, embedding the loop resonator reduces radiation losses of the resonator. The design of the vertical-coupling section requires two important considerations. Firstly, the 50Ω impedance level has to be maintained throughout the loop, and secondly, the coupling coefficient obtained will correlate with the bandwidth of the filter. Figures 5.3(a) and 5.3(b) show the vertical

coupling section and the corresponding directional filter respectively.

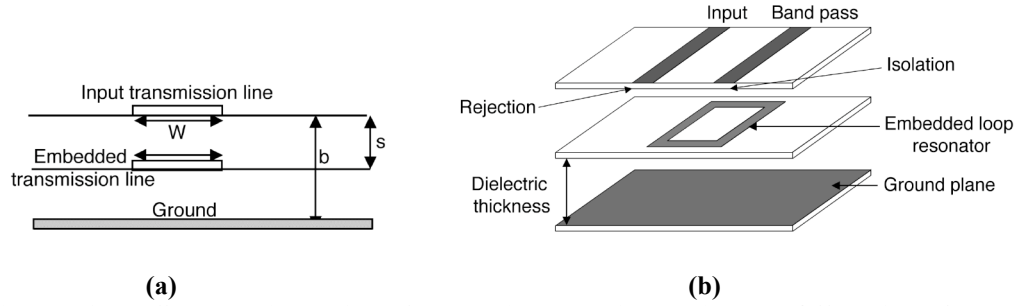


Figure 5.3. (a) Cross-sectional view of the vertical-coupling section; (b) Offset view of the structure of the directional filter.

To obtain the maximum coupling and minimum insertion loss, only one dielectric layer is inserted in between two successive metal layers. Hence s and b (shown in figure 5.3(a)) have values of $100\ \mu\text{m}$ and $200\ \mu\text{m}$ respectively. Figure 5.4 shows the top view of the vertical coupling section where the input transmission line and the embedded transmission line in the coupled section are completely overlapped for the maximum possible coupling.

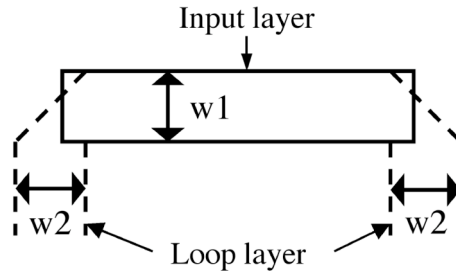


Figure 5.4. Top view of the vertical-coupling section.

The value of w_2 ($125\ \mu\text{m}$) corresponds to the width of the $50\ \Omega$ embedded microstrip transmission line in the loop layer. The value of w_1 should correspond to a $50\ \Omega$ -coupled section to preserve the $50\ \Omega$ impedance level in the loop. Hence, the look-in reflection coefficient of the $\lambda_g/4$ -coupled section as seen from the embedded loop layer has been minimized to obtain the value of w_1 . Figure 5.5 shows the simulated reflection

coefficient (as seen from the loop layer) and the coupling of the coupled section with the variation of w_1 at our frequency of interest (40 GHz).

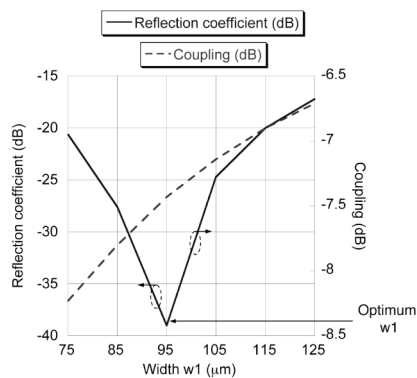


Figure 5.5. Variation of the simulated reflection coefficient and coupling coefficient of the coupled section with w_1 .

The optimum w_1 to minimize the reflection coefficient is determined as 95 μm , and the corresponding coupling is 7.43 dB. That corresponds to 6.3% fractional bandwidth [34]. The effective length of coupled sections is 810 μm , which corresponds to the $\lambda_g/4$ wavelength in the embedded loop layer. Lengths of non-coupled sections of the loop are 830 μm , which corresponds to the $\lambda_g/4$ wavelength of the embedded microstrip line in the loop layer.

The overall design occupies an area of $1.7 \times 1.7 \text{ mm}^2$ for the 40 GHz passband frequency. The insertion loss, rejection and isolation have been derived from the multiple sets of two port measurements on the same device. A TRL (thru-reflect-line) deembedding scheme is incorporated to deembed the effect of probe pads in all measurements. Figure 5.6 shows the fabricated directional filter library on the multilayer LTCC substrate.

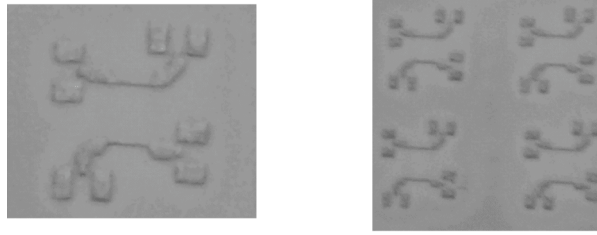


Figure 5.6. Photograph of fabricated directional filter library in multilayer LTCC substrate.

Measurement results show 2.82 dB insertion loss at the center frequency of 38.1 GHz with a 6.3% 3-dB fractional bandwidth. The maximum rejection is 15.3 dB, and the isolation is higher than 11 dB (maximum 23 dB) in the frequency band. The reflection is approximately 20 dB in the entire frequency band. The 5 % shift in the center frequency is attributed to the dielectric-constant variation. Figure 5.7 shows the EM-simulated and the measured performance of the directional filter. It shows a good match between the simulated and the measured result. But as graphs indicate, the directional filter does not have the rejection, reflection, and isolation minima at the same frequency. This is due to different phase velocities of the input transmission line and the embedded transmission line in the vertically coupled section. Hence, directional filter's characteristics are imbalanced as indicated in Figure 5.7. Also, widths of all transmission lines are comparable to their lengths. So the difficulty in determining the effective lengths of transmission lines adds up to the degradation of performance. Other possible vertical-coupling schemes are investigated in the subsequent sections to address this aspect.

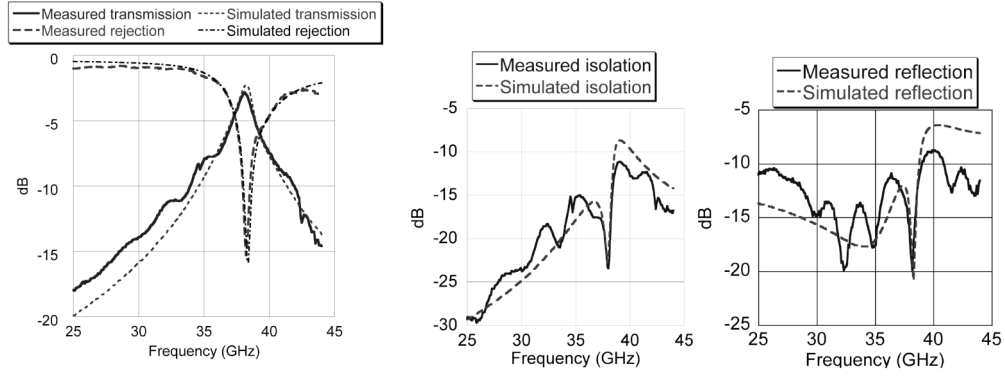


Figure 5.7. Simulated and measured performance of the directional filter.

5.2.1.3 Different vertical-coupling implementations

Two different vertical-coupling structures are considered to separately optimize the reflection and isolation characteristics. Figure 5.8(a) shows the vertical coupling structure where different widths of the coupled transmission lines have been used in the different layers. Hence, it is named as asymmetrically coupled directional filter. Figure 5.8(b) shows a reduced vertical coupling, as there is no overlap between the input transmission line and the embedded transmission line.

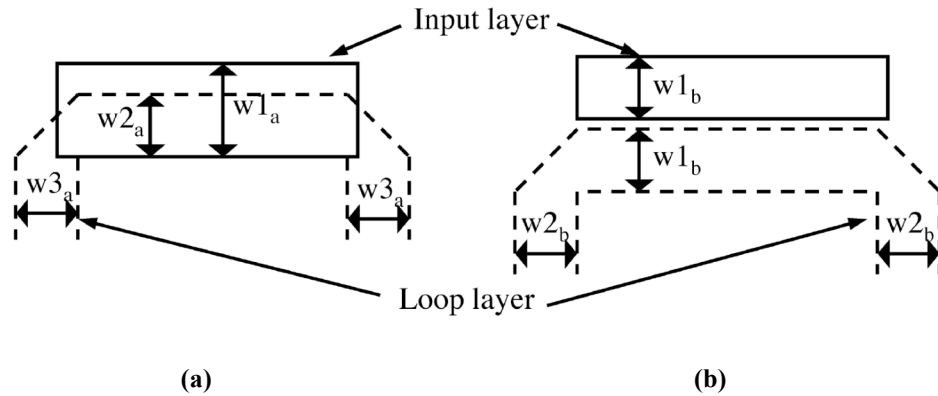


Figure 5.8. (a) Asymmetric-vertical-coupling structure; (b) Reduced-vertical-coupling structure.

To minimize the number of design variables in the case (a), $w1_a$ ($=285 \mu\text{m}$) and $w3_a$ ($=125 \mu\text{m}$) have been fixed as the width of the 50Ω transmission line in the input metal

layer and the loop layer respectively. w_{2a} is chosen as $95 \mu\text{m}$ because it corresponds to the minimum simulated reflection coefficient of the coupled section as seen from the loop (same procedure as given in Figure 5.5). This approach maintains the 50Ω impedance level throughout the loop, and corresponds to a simulated coupling of 7.48 dB, which in turn predicts 6.25 % 3-dB fractional bandwidth [34].

In the case (b), w_{2b} ($=125 \mu\text{m}$) has been fixed as the width of the 50Ω transmission line in the embedded loop layer. w_{1b} ($=105 \mu\text{m}$) minimizes the look-in reflection coefficient of the coupled section as seen from the loop. This corresponds to a coupling coefficient of 9 dB that predicts 4.3% fractional bandwidth [34].

Figure 5.9 shows the measured performance of the cases (a) and (b) respectively. Table 5.1 summarizes the performance of these directional filters.

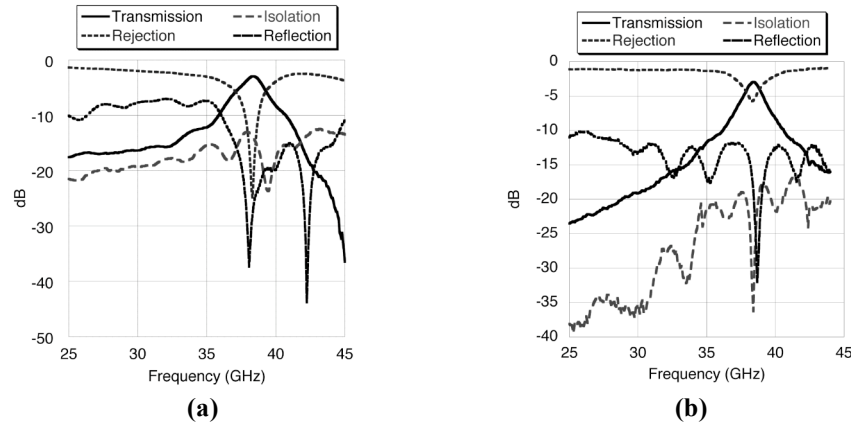


Figure 5.9. (a) Measured performance of the asymmetric-vertical-coupling directional filter; (b) Measured performance of the reduced-vertical-coupling directional filter.

Table 5.1. Performance comparison of different vertical-coupling schemes.						
	Center frequency (GHz)	Insertion loss (dB)	Bandwidth (GHz)	Rejection (dB)	Isolation (dB)	Reflection (dB)
Asymmetric coupling	38.4	2.9	2.35	22	13-15	> 25
Reduced coupling	38.4	2.93	1.8	5.75	~25	> 20

5.2.1.4 Performance optimization of the directional filter

The optimization of the vertical coupling section alone could not generate the optimum performance as indicated by the performance of the previous directional filters. Also, the different performance optimums do not overlap in these two cases. Hence, another design parameter L is introduced as shown in the Figure 5.10. This leads to a rectangular loop instead of the conventional square loop. In this figure, L_1 ($=810\text{ }\mu\text{m}$) & L_2 ($=830\text{ }\mu\text{m}$) denotes the effective length of the $\lambda_g/4$ transmission line in the loop layer in the coupled section and the non-coupled section respectively.

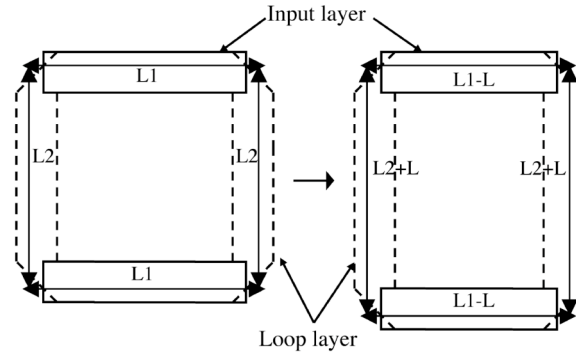


Figure 5.10. Optimization of directional filter structure to improve the overall characteristics.

Using this technique, optimum frequencies of the band rejection, isolation, and reflection can be controlled with the variation in L , and different values of L reflect different performance optimums. This technique is applied on the symmetrically and strongly coupled directional filter (shown in figure 5.4) as its performance is inherently the most balanced one. Figure 5.11 shows the simulated variation of the isolation, reflection, and rejection at the center frequency (40 GHz).

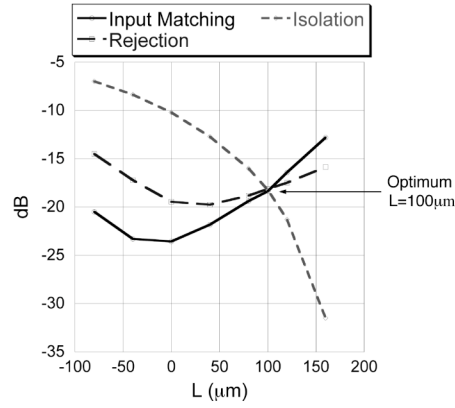


Figure 5.11. Variation of the isolation, reflection, and band-rejection of the directional filter at the center frequency with L.

This figure shows that the increase in L improves the isolation characteristics, and the reduction in L enhances the reflection and rejection characteristics. Hence, we cannot obtain the optimum of the all of them for a single value of L . We estimate L ($=100 \mu\text{m}$) to obtain an acceptable minima of performance parameters, and so the insertion loss is minimized. Figure 5.12 shows the simulated and measured performance of the optimized rectangular loop directional filter. It has an insertion loss of 2.25 dB at the center frequency of 38.5 GHz with 6.1 % 3-dB fractional bandwidth (2.35 GHz). It shows a band rejection of 16 dB at the center frequency, and has a higher than 15 dB isolation throughout the frequency band (maximum 23 dB). The reflection is better than 20 dB at the center frequency. Table 5.2 summarizes the performance of the directional filter before and after the optimization procedure. The optimization technique improves the insertion loss by approximately 0.6 dB, rejection by 1 dB, and isolation by 4 dB. Furthermore the resultant performance is symmetric and comparable to ideal edge-coupled directional filter performance.

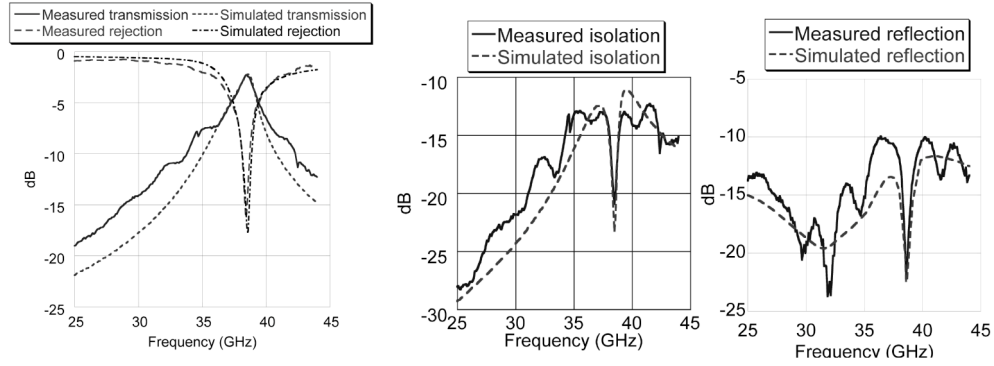


Figure 5.12. Simulated and measured performance of the optimized directional filter.

Table 5.2. Performance comparison of the directional filter optimization.					
	Center frequency (GHz)	Insertion loss (dB)	Band-width (GHz)	Rejection (dB)	Isolation (dB)
Square loop	38.1	2.82	2.4	15.3	> 11
Rectangular loop	38.5	2.25	2.35	16.3	> 15

5.2.2 Directional filter-based multiplexer

Directional filters can be cascaded for multiplexing and demultiplexing operations as shown in Figure 5.13. The first directional filter presents a pass band at frequency f_1 , and the second one presents a pass band at frequency f_2 . This enables the use of directional filters in millimeter-wave multi-band applications.

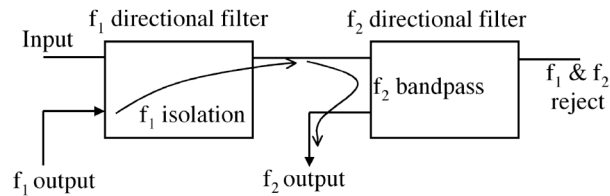


Figure 5.13. Directional filter-based demultiplexing/multiplexing and leakage path between outputs.

Two loop resonators at different frequencies are sequentially coupled to the signal path to realize the multi-band operation. The isolation between outputs of the multiplexer is critical in this design and is described in Figure 5.13. It depends on the isolation path of the first directional filter and the bandpass path of the second directional filter. To improve the overall isolation, the isolation of the f_1 directional filter has to be high. Previous implementations of directional filters indicate that the filter with reduced coupling between the input transmission line and the loop (shown in Figure 5.8(b)) provide maximum isolation (approximately 10 dB higher than others). Hence this reduced-vertical-coupling scheme has been chosen for the loop resonating at f_1 as shown in Figure 5.14.

Multiplexers are designed to have passbands at 32 GHz/40 GHz and 36 GHz/40 GHz respectively with approximately 5 % fractional bandwidth in each band following the previous directional filter design procedures. Dotted lines in Figure 5.14 denote the embedded loop layer, and continuous lines denote the transmission line in the top metal layer. The width of the input transmission line is kept same for both coupling sections to minimize discontinuities, and widths of the coupled section of the loops are adjusted to minimize the look-in reflection coefficients of the respective coupled sections.

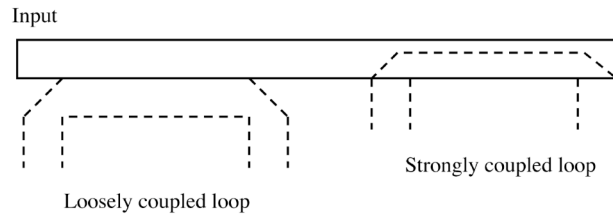


Figure 5.14. Coupling sections of the multiplexer.

Figure 5.15 shows the photograph of fabricated LTCC multiplexers. Multiple two-

port measurements have been performed with two other ports terminated with broadband loads to determine the insertion loss in each passband and the isolation between them. Figure 5.16 reports the measured performance of multiplexers. Table 5.3 summarizes the performance of the different multiplexers.

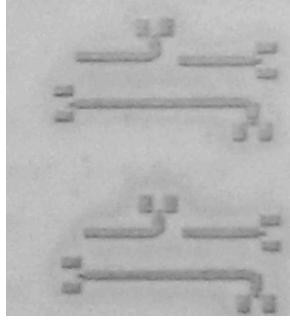


Figure 5.15. Photograph of fabricated multiplexers in LTCC process.

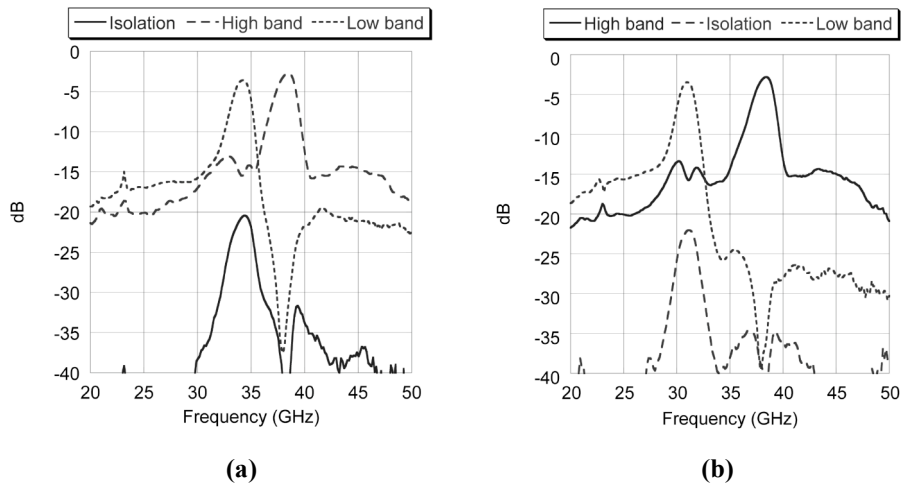


Figure 5.16. (a) Measured performance of the 4 GHz-band-separation multiplexer; (b) Measured performance of the 8 GHz-band-separation multiplexer.

Table 5.3. Performance summary of multiplexers.				
Band separation (GHz)	Center frequency (GHz)	Band-width (GHz)	Insertion loss (dB)	Minimum isolation (dB)
4	34.3/38.5	1.8/2.15	3.58/2.72	20.4
8	31/38.5	1.65/2.15	3.4/2.78	22.3

Both multiplexers show higher than 20 dB isolation between outputs. Such isolation is suitable for the multi-band operations. Both of them show around 3 dB insertion loss in the passbands with 5.2 %-5.6 % fractional bandwidth. Hence, multiplexers demonstrate an excellent potential for the millimeter-wave multi-band system realization. However the spurious of the higher frequency loop at the lower pass-band frequency (maximum 12.5 dB for 4 GHz separation and 13.7 dB for 8 GHz separation) limits the minimum band separation for the single-loop implementations. Higher order filters should be implemented for better suppression of the spurious response at smaller band separations.

To summarize, an extremely useful passive multi-band multiplexing/demultiplexing scheme has been demonstrated using directional filter as the basic building block. A systematic design procedure is developed for directional filter and multiplexer implementation, and an optimization procedure has been developed.

5.3 Millimeter-wave tunable amplifier development

This section demonstrates, for the first time, a silicon-based millimeter-wave frequency-tunable amplifier. First, a phase-tunable transmission line is demonstrated using an on-chip multi-metal-layer topology. Next, a frequency-tunable multi-band amplifier is presented with that tunable transmission line in the output-matching network. Measured results of the amplifier indicate center frequencies at 25 GHz and 32 GHz under two different control conditions with more than 10 dB power gain at each frequency band.

There has been a demonstration of a tunable millimeter-wave amplifier in 0.2 μm GaAs pseudomorphic-high-electron-mobility-transistor (pHEMT) process by manipulating the length of an open stub [59]. However, that tunable approach uses irreversible air-bridges, and does not provide balanced gain over different frequency bands. In another demonstration [60], a tunable transmission line is shown to change the phase of a transmission line by using a variable floating/ground metal between the signal line and the ground plane. This tunable approach is utilized in the subsequent sections to develop the millimeter-wave tunable amplifier.

5.3.1 Tunable transmission line in 0.18 μm SiGe

The tunable transmission line (TL) is implemented using M7 (top metal) as signal line, M6 as the variable floating/ground line directly under M7 signal line, and M1 (bottom metal) as the ground plane in a 7-metal layer 0.18 μm SiGe process. The microstrip configuration is chosen for the transmission line, so that the phase shifting by vertical coupling with another metal line is maximized. In addition, the closest metal

layer (M6) is used as the variable floating/ground line to increase the phase difference between the two modes as explained later. The schematic of the tunable TL is shown in Figure 5.17.

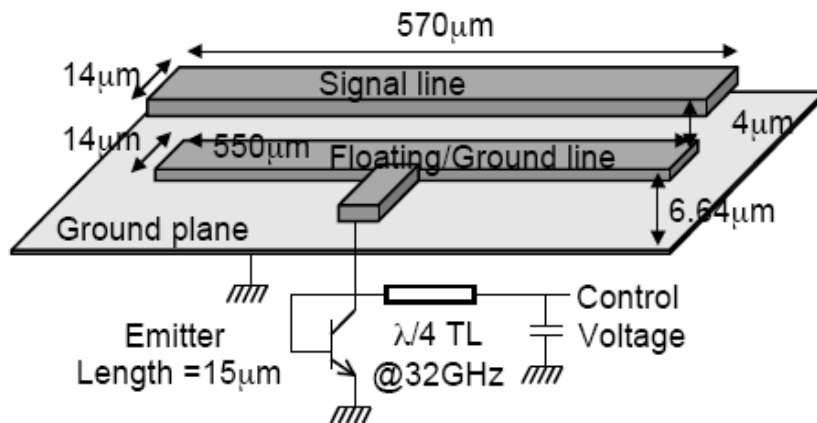


Figure 5.17. Structure of the tunable TL.

When floating, the M6 metal line vertically couples with the M7 signal line. However, the coupling is weak, and hence, the insertion loss of the transmission line is not affected much at the operating frequency range. When grounded, the M6 metal line acts as the ground plane for the M7 signal line. Hence, the M7 signal line becomes much more capacitive in nature, modifying the propagation constant leading to an increase in the phase shift [34]. In this particular implementation of the tunable transmission line, the width of the M6 line is chosen same as the M7 signal line. Their width corresponds to the $50\ \Omega$ M7 signal line in the absence of the M6 line so that there is no discontinuity between the tunable TL and the other TLs in the output-matching network of the amplifier. The choice of relative width between M6 line and M7 line is the trade-off between a larger phase shift of the TL at one operating condition (a wider M6 line would cause a higher phase-shift because of higher capacitance at ground state of M6 line), and a worse performance of the TL at another operating condition (a wider M6 line in

floating state would couple more to the M7 signal line causing a higher insertion loss of the M7 signal line). A base-collector shorted n-p-n transistor (emitter length = 15 μm) is used as a diode connected to the M6 line. The $\lambda/4$ TL isolates the diode with the external power supply at frequencies around 32 GHz. When the control voltage is 0 V, the diode is off, and hence the intermediate M6 line is in the floating state. When the control voltage is 1 V, i.e., much higher than the turn-on voltage of the diode, the diode is on consuming 12 mA of DC current. In this condition, the diode presents a very small series resistance across its terminals. The emitter of the diode and the ground plane are in the same potential as shown in Figure 5.1. Hence, the M6 line acts as a ground line.

The EM simulator used to predict the performance of the TL is IE3D. The simulated and the measured performance of the tunable TL are shown in Figure 5.18. Measured results show approximately 20 degrees phase difference between two modes of operation over 20 GHz-40 GHz frequency range. In addition, the insertion loss at 1 V control voltage is less than 2 dB till 30 GHz, and the insertion loss at 0 V control voltage is around 1 dB in 25 GHz-40 GHz frequency range. The slight mismatch between the measured and simulated TL performance can be attributed to the non-ideal behavior of the diode switch, i.e., the diode does not present a perfect open at off state, and also does not present a perfect short at on state. Figure 5.19 shows the die photograph of the tunable TL test structure.

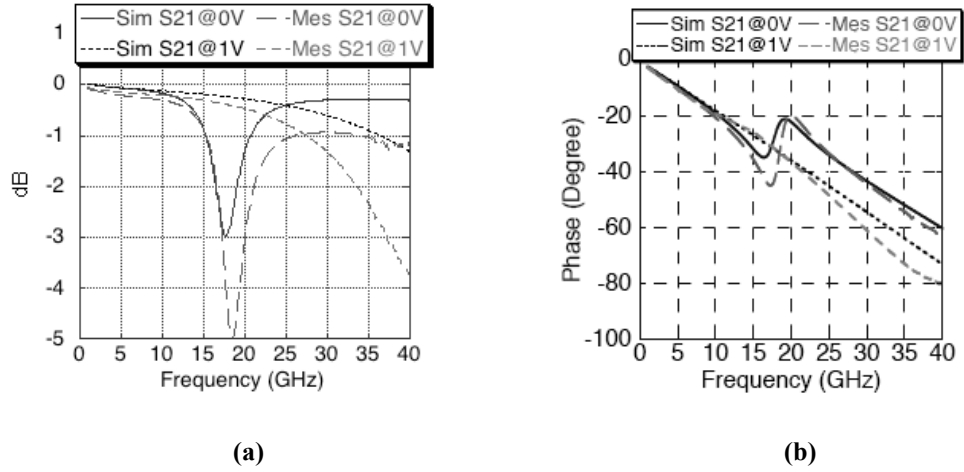


Figure 5.18. (a) Measured and simulated insertion loss of the tunable TL; (b) Measured and simulated phase of the tunable TL.

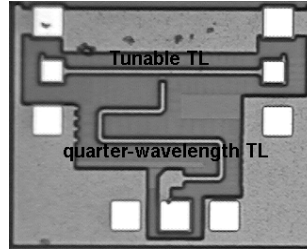


Figure 5.19. Die photograph of the tunable TL test structure.

5.3.2 Tunable amplifier in 0.18 μm SiGe

A cascode amplifier is designed with the tunable transmission line in the output-matching network. The input matching of the amplifier is inherently broadband in nature, and hence, can cover both the frequency bands achievable by tuning the output-matching network. A 6 μm emitter length is used for the n-p-n HBT transistors. Figure 5.20 shows the schematic of the amplifier. The tunable transmission line is used in the output-matching network to shift the matching frequency by approximately 25%. The nominal matching-network design has been performed at the higher frequency band to balance the gain of two operational modes. The other TLs are microstrip 50 Ω lines with M7 signal and M1 ground plane. The die photograph of the tunable amplifier is shown in Figure

5.21. The die area is 1.65 mm × 0.67 mm.

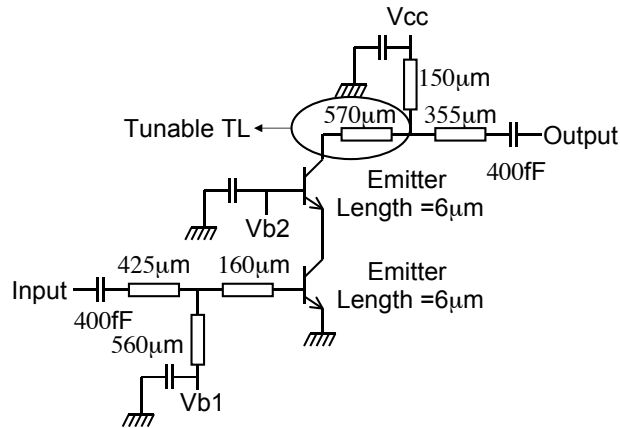


Figure 5.20. Schematic of the tunable cascode amplifier.

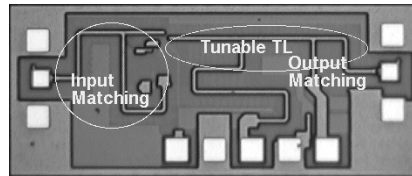


Figure 5.21. Die photograph of the fabricated tunable cascode amplifier.

Measured s-parameters are shown in Figure 5.22 along with simulated results. Measured results indicate higher than 10 dB gains in both frequency bands (at 25 GHz and 32 GHz center frequencies) with less than 0.4 dB of gain imbalance between the bands. The measured 1-dB bandwidth is higher than 5.4 GHz and 8.8 GHz in the lower and higher frequency band respectively, and these bandwidths overlap with each other. The measured output matching is better than 20 dB at 27 GHz (control voltage of the tunable TL=1 V), and the measured output matching is better than 10 dB at 33 GHz (control voltage of the tunable TL=0 V). The measured input matching is broadband (higher than 15 dB from 20 GHz-50 GHz). The amplifier core consumes 16.5 mW (5 mA from 3.3 V supply), and the diode switch consumes 12 mW when the control voltage is 1 V (0 mW at off state).

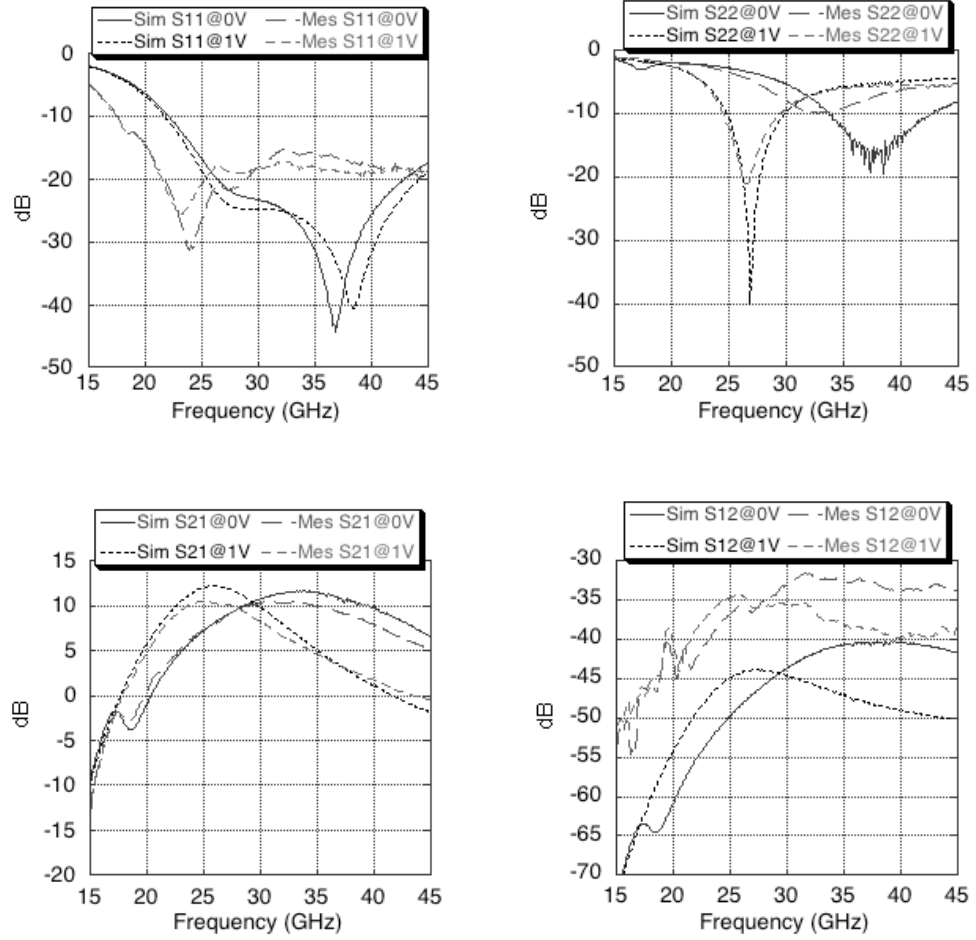


Figure 5.22. Measured and simulated s-parameters of the tunable cascode amplifier.

The tunable amplifier presents an excellent opportunity for millimeter-wave multi-band or cognitive wireless systems. The tunability and the frequency shift of this approach can be extended by using more tunable transmission-line sections at different stages of matching networks.

5.4 Summary

Demonstrations of different filtering and amplifier solutions have been presented in this chapter towards the future multi-band and cognitive millimeter-wave systems. The directional filter-based multiplexing solution presents a SOP integration approach with the frequency band selection capabilities. A systematic design procedure has been presented for vertical-coupling implementation of directional filters with different performance optimums. The optimized directional filter is measured to have an insertion loss of only 2.25 dB at 38.5 GHz center frequency with 2.35 GHz 3-dB bandwidth. Resultant multiplexers demonstrate approximately 3 dB insertion loss in each band (separated by 4 GHz and 8 GHz) with at least 20 dB isolation between them.

The tunable amplifier developed in 0.18 μm SiGe process provides a generic approach for tunable multi-band amplifiers by tuning the phase of the transmission-line elements in the matching network. A base-collector shorted npn HBT (in diode configuration) switches the intermediate metal line between the floating and the ground state to realize the phase tunability of the transmission line. A phase difference of 20 degrees is measured in two different states of the tunable transmission line over 20 GHz-40 GHz frequency range due to the variation in the propagation velocity. This tunable TL is utilized in the output matching of the cascode amplifier to switch the output-matching frequency between 27 GHz and 33 GHz. The amplifier shows a measured balanced gain of higher than 10 dB at two different frequency bands at 25 GHz and 32 GHz.

Chapter 6

Conclusions and Future Work

6.1 Technical contributions

In this dissertation, the development of integrated silicon-based 60 GHz receiver front-end is demonstrated. The goal of the research is to demonstrate ultra high-speed, low-power, and compact integrated wireless communication devices operating at 60 GHz wireless-transmission frequency. The implemented 60 GHz receiver front-end can support up to 10-15 Gbps wireless data transmission depending on the modulation scheme used. The front-end is extremely low power, and suitable for single-chip integration for portable wireless applications. A low-cost technique of integrating the silicon-based ICs on the packaging substrate is also demonstrated. Finally, different building blocks towards the realization of the multi-band and cognitive millimeter-wave systems are presented. The specific technical contributions and summary related to different aspects of the research are summarized next in this section.

In the second chapter, the evolution of millimeter-wave IC and packaging technologies is shown towards a very compact, portable solution integrable into consumer wireless products starting from large millimeter-wave modules for space and radar communications. A detailed study of the possible heterodyne and homodyne system architectures is presented with the focus on 60 GHz integrated receiver front-end

development. The system parameters, i.e., link margin, sensitivity, and dynamic range are investigated for different modulation schemes and antenna implementations. It has been shown that a wireless-link distance of 2-5 m with simple architectures (small antenna array and compact low-power integrated silicon-based IC), and a link distance of greater than 10 m with phased array architectures can be realized. Finally, a hybrid system-integration methodology has been presented demonstrating multi-gigabit transmission at 60 GHz. This hybrid integrated approach serves as the bridge between the traditional millimeter-wave modules and the integrated, portable approach focused in this dissertation. A 4X subharmonic mixing has been presented using low-cost organic substrate and GaAs anti-parallel diode pair. Two back-to-back subharmonic mixers show simultaneous modulation and demodulation of up to 1.5 Gbps digital data. This hybrid implementation demonstrates that the low-cost organic packaging schemes can be efficiently used at 60 GHz.

In the third chapter, a low-power architecture for the development of 60 GHz receiver front-end is demonstrated using low-cost 130 GHz f_T 0.18 μm SiGe process, i.e., much lower cost compared to the state-of-the-art 220 GHz f_T 0.12 μm SiGe process. . In order to realize the receiver front-end, a high-gain cascode amplifier is implemented using a novel gain-boosting technique to overcome the performance limitations of the process. The implemented gain-boosting technique increases the gain of a single cascode stage by more than 4 dB for a lower DC power consumption. The front-end amplifier is measured to have a gain of 24 dB with 4 GHz 3-dB bandwidth for only 25 mW DC power consumption.

Two different receiver architectures suitable for the low-cost process are implemented. The first receiver implementation is a non-coherent amplitude-detection scheme integrated with a low-cost organic package. This integrated receiver demonstrates an extremely low power budget of 25 pJ/bit for a multi-gigabit data transmission over the wireless link up to 2 meters of distance. A complete antenna-to-demodulated-baseband solution is integrated in this particular approach. This is the *first report* of a non-coherent 60 GHz receiver front-end integration in 0.18 μm SiGe with the *lowest reported* power budget to date for 60 GHz receivers.

A subharmonic 60 GHz front-end is also demonstrated *for the first time* using low-cost 0.18 μm SiGe. The 2X subharmonic mixing is shown to have broadband characteristics, and is measured to have the minimum conversion loss among the reported publications of subharmonic mixing based on anti-parallel diode pair. The front-end (three-stage LNA + 2X subharmonic mixer) provides a conversion gain of 16 dB with 4 GHz RF bandwidth for only 27 mW DC power consumption. Another version front-end integrated with the on-chip oscillator shows similar conversion performance.

However, the application of such a low-cost low-power SiGe front-end is still limited by the integration of digital baseband processors. A complex true baseband processing (traditionally all CMOS) scheme with multi-Gbps throughput is extremely challenging in a 0.18 μm process. In addition, the amplitude-detection scheme or the subharmonic front-end demonstrated in this chapter cannot scale to a 10 Gbps throughput because of limited front-end bandwidth available (3-4 GHz instead of full 7 GHz), limitation in terms of application modulation schemes (QPSK realization is extremely challenging in direct-conversion, and for heterodyne scheme, a high-throughput QPSK would require a IF of at

least 6 GHz i.e., twice the data rate in each channel). Hence, a high-throughput solution requires a better performance IC process suitable for low-cost digital integration, i.e., traditional CMOS.

In order to develop the receiver front-end, a systematic characterization of both passive and active devices are performed in the 90 nm CMOS process. A front-end two-stage LNA is developed cascading two cascode amplifier stages. The LNA provides 15.5 dB gain for a DC power consumption of 29 mW. The 1-dB bandwidth is 59.3 GHz – 65 GHz. The measured noise figure is approximately 6-7 dB in the entire frequency band. The front-end LNA demonstrates the highest-gain with a very accurate and wideband frequency characteristics among the reported CMOS LNAs.

Two different types of mixers are implemented to accommodate different heterodyne solutions. The LO rejection is implemented in the subsequent IF stages for both the mixers. A double-gate mixer is implemented with a single-ended LO power requirement of –2 dBm. The IF output of the double-gate mixer is single-ended. Hence, an IF single-ended-to-differential converter is required to generate a differential IF output. On the other hand, a single-ended Gilbertcell mixer is implemented with approximately –4 dBm differential LO power requirement. Different versions of the wideband front-end are investigated and implemented. A front-end gain of 23.5 dB (30.5 dB for capacitive loading of the second down-conversion mixer) is demonstrated for an IF bandwidth of 6.5 GHz – 12.5 GHz, i.e., a RF bandwidth of 57.5 GHz – 63.5 GHz, for only 75 mW of DC power consumption. A modified version of the front-end provides 34 dB gain for 4 GHz – 12 GHz IF bandwidth. These are the most wideband demonstrations of the receiver front-end in CMOS processes.

Table 6.1 compares the implemented SiGe receivers and CMOS receivers in this work with the other reported SiGe and CMOS receiver front-ends.

Table 6.1 Performance comparison of silicon-based 60 GHz receiver front-ends.						
Process [ref]	RF frequency (GHz)	Conversion Gain (dB)	RF bandwidth (GHz)	DC power (mW)	Input P1-dB (dBm)	Noise figure (dB)
0.12 μm SiGe [19]	60	40 (includes second down-conversion)	6	~ 324 mW (with baseband buffer, without PLL)	-36	5-6.7
0.13 μm CMOS [25]	60	11.8	6	77 mW (with VCO)	-15.8	10.4
90 nm CMOS [24]	53	26-31.5 (includes second down-conversion)	NA	80 mW	-25.5	6.9-8.3
0.18 μm SiGe ASK [this work]	60	24 dB from LNA + 4 dB from baseband buffer (gain of amplitude detector is dependent on input signal)	3	37 mW (from antenna to demodulated baseband)	NA (ASK demodulation)	8-9
0.18 μm SiGe subharmonic [this work]	60	16.5	4	27 mW (62 mW with VCO)	-37	8-9
90 nm CMOS heterodyne [this work]	60	23.5 (31 dB with capacitive loading)	6 (8 in another version)	70 mW (without VCO)	-22.5 dBm (-30 with capacitive loading)	7-8

From this comparison table, we can see the implemented 0.18 μm SiGe front-ends are extremely suitable for low-power low-cost direct-conversion applications up to 3-4 Gbps throughput, and their performance is comparable to the more advanced processes. The implemented 90 nm heterodyne front-end is suitable for wideband high-gain front-end.

Another version of the implemented 90 nm heterodyne front-end provides 8 GHz RF bandwidth with 34 dB gain for 82 mW DC power consumption. This is the most wideband implementation among 60 GHz front-ends. Hence, the proposed CMOS 60 GHz solution promises a very high data rate (> 10 Gbps). Also, high-speed digital processing and baseband circuitry can be realized using 90 nm CMOS. Hence, a single-chip CMOS 60 GHz transceiver solution is promised.

In the fifth chapter, different building blocks for millimeter-wave multi-band and tunable systems are demonstrated. The directional filter-based multiplexing solution presents a SOP-integration approach with the frequency band selection capabilities. The optimized directional filter is measured to have an insertion loss of only 2.25 dB at 38.5 GHz center frequency with 2.35 GHz 3-dB bandwidth. Resultant multiplexers demonstrate approximately 3 dB insertion loss in each band (separated by 4 GHz and 8 GHz) with at least 20 dB isolation between them.

The tunable amplifier developed in 0.18 μm SiGe process provides a generic approach for tunable multi-band amplifiers by tuning the phase of the transmission-line elements in the matching network. A base-collector-shortened npn HBT (in diode configuration) switches the intermediate metal line between the floating and the ground state. A phase difference of 20 degrees is measured in two different states of the tunable transmission line over 20 GHz-40 GHz frequency range due to the variation in the propagation velocity. This tunable TL is utilized in the output matching of the cascode amplifier to switch the output-matching frequency between 27GHz and 33GHz. The amplifier shows a measured balanced gain of higher than 10 dB at two different

frequency bands at 25 GHz and 32 GHz. This is the first reported demonstration of such a tunable amplifier scheme at millimeter-wave frequencies.

6.2 Future work

The 60 GHz wireless communication scheme presents an excellent opportunity in terms of a low-power, low-cost, ultra-high data rate, integrated, and portable communication device. These aspects are demonstrated in this dissertation through the development of key building blocks and millimeter-wave integrated receiver solutions. The future application of this research is the picture shown in Figure 6.1.



Figure 6.1. Video and data-transfer applications of 60 GHz radios.

The future work in terms of 60 GHz radios involves the practical implementation of portable consumer devices for these applications. A proper convergence of low-cost module development, low-cost and low-power millimeter-wave IC development, and low-power baseband signal processing is necessary for the meaningful integrated 60 GHz solution. In this section, further challenges for such an implementation and possible solutions are discussed.

6.2.1 CMOS 60 GHz phased-array receiver

Figure 2.9 demonstrated the possible wireless link distance for different link margins. According to that figure, a line-of-sight (LOS) link distance of 2-5 m is achievable with acceptable SNR (the data rate would depend on the modulation scheme used) and single-antenna configuration. However, the high absorption of the 60 GHz signals by objects as well as human beings would require the phased-array implementation for non-line-of-sight (nLOS) applications for a longer wireless link distance. Phased-array systems, a special case of multiple-input-multiple-output (MIMO) systems, take advantage of spatial directivity and array gain to increase spectral efficiency [61]. Phased array systems can form beams and nulls in desired directions by controlling the time delay and gain of the signal in each path independently.

It is essential to develop small form-factor antennas on organic substrates to develop 60 GHz modules opposed to the traditional large phased array radars. Theoretically, different phased-array architectures are possible: i) direct phase-shift in RF signal path using millimeter-wave phase shifter, ii) IF phase-shifting, iii) LO phase-shifting, and iv) phase-shifting in digital domain. As a trade-off between power consumption, die area, and performance, LO-path phase shifting seem to be a possible solution for silicon-based IC processes [62]. An integrated CMOS millimeter-wave phased-array solution would provide much flexibility and robustness in terms of high-speed multi-Gbps wireless applications. The most critical challenges for such an implementation are scalability, compactness, power consumption, and phase-shifter implementation.

6.2.2 CMOS 60 GHz multi-channel receiver architecture

A multi-channel architecture is suitable to handle the large 7 GHz bandwidth of the 60 GHz frequency band. Presently, in the standard bodies (IEEE 802.15.3c and ECMA), proper channelization methods are discussed to develop a meaningful solution for baseband processing, synchronization techniques, and modulation schemes. However, it is critical to modify the 60 GHz receiver front-end according to the multi-channel schemes towards the development of tunable IF amplifier architecture or interference-free baseband demodulation techniques. This would be an active area of research in future.

6.2.3 Cognitive and multi-band millimeter-wave front-end

In the long-term future, there is enough potential for the integration of available millimeter-wave front-ends into a single multi-band front-end chipset with possible cognitive or tunable elements. Such a chipset would be able to address issues regarding various application scenarios and enhance the performance. An early investigation towards the implementation of the multi-band and tunable millimeter-wave elements, presented in chapter 5, promises the possibility of such an implementation. However, this idea needs to address different challenges with respect to actual implementation of tunable/multi-band millimeter-wave elements, frequency planning, synchronization, and antenna development.

6.2.4 Conclusion

The last decade has seen a tremendous development of cellphone architectures, from early voice-handsets to present cellphones with data, multi-media, and computing applications. The next decade would observe a translation in the millimeter-wave applications, from primarily costly military and space domain, to low-cost small form-factor consumer application devices, with a potential that is one order of magnitude higher than the present devices. *The next wireless wave is going to be millimeter-wave* [52] with a significant focus on 60 GHz multi-Gbps applications.

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Invention Disclosures

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Vita

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